Abstract: Motion-Aware Reconfigurable Computing for H.264/AVC Motion Estimation Algorithm

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Abstract

In this paper, we propose an approach for motion-aware reconfigurable architecture to perform H.264/AVC Variable Block Size Motion Estimation (VBSME) algorithm. We show that by adaptively adjusting the search range on the reconfigurable hardware platform, the computational cost of motion estimation required for interframe encoding with H.264/AVC video compression standard can be reduced significantly. Therefore, the hardware resources used can be configured adaptively with the search range specifications through dynamic partial reconfiguration to make best use of hardware resources and power during runtime. A scalable SAD array is proposed which can perform full search block matching algorithm for integer pixel Motion Estimation of smaller 4x4 blocks. The implemented architecture can support real time applications with various resolutions and frame rates at a maximum frequency of 90 MHz.

Acknowledgements
This work was supported by the Hongik University new faculty research support fund.