10 nm Si pillars fabricated using electron-beam lithography, reactive ion etching, and HF etching

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(Received 21 June 1993; accepted 30 July 1993)

This article reports the fabrication and preliminary photoluminescence (PL) study of free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15. The pillars were fabricated using electron-beam lithography, chlorine based reactive ion etching (RIE), and subsequent HF wet etching. Using HF etching offers several advantages: (a) it is a relatively stress independent process and therefore preserves the original shape of the structure; (b) it is a room temperature process; (c) it has a very controllable etch rate, ~1.9 nm/h; and (d) it can remove RIE damage and passivate the Si surface. PL with a peak at 720 nm was repeatedly observed from an array of nanoscale pillars with ~20 nm diameters. However, the cause of such PL is still unclear.

I. INTRODUCTION

The ability to fabricate nanoscale pillars in Si in a very controllable way is of great interest to many fields, such as quantum effect Si devices, nanoscale sensors, and field emitters, just to name a few. Another attractive aspect of such fabrication is the possibility to shed light on the origin of photoluminescence (PL) from porous Si.[1] To date, the PL has been explained in terms of quantum confinement,[2] and surface chemistry.[3]

Previously, oxidation techniques have been employed to further reduce the size of silicon pillars for fabricating field emitters and microsensors,[4] and for studying luminescence.[5] The oxidation process has two drawbacks. First, it is a stress dependent process, therefore is nonuniform and significantly changes the original shape of the pillars. Second, it is a high temperature process which could pose problems in some applications.

In this article we present a different approach to fabricating free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15. The process utilizes electron beam lithography, chlorine-based reactive ion etching (RIE), and subsequent HF wet etching. HF etching offers several advantages. First, HF etching is a relatively stress independent process and therefore preserves the original shape of the structure. Second, it is a room temperature process, making it a much more versatile process than high temperature oxidation. Third, it has a very controllable etch rate, ~1.9 nm/h. And finally, it can remove RIE damage and passivate the Si surface. A preliminary investigation of PL from the nanoscale Si pillars is also presented.

II. FABRICATION

The 10 nm Si pillar fabrication process consists of three main steps: etch mask definition, RIE, and HF etching to reduce the size of the pillars. All experiments were performed on 3–12 Ω cm *p*-type (100) Si wafers. The Cr etch masks were defined using electron beam lithography and a lift-off process. Electron-beam lithography was performed using a modified scanning electron microscope (SEM), described elsewhere,[6] operated at 35 kV. Arrays of dots were exposed in 950 K polymethylmethacrylate (PMMA), 70 nm thick on top of the Si substrate, and developed in a mixture of 2-ethoxyethanol and methanol. After development, 40 nm of Cr was evaporated onto the samples. A lift-off process left arrays of Cr dots which were used as the etch mask for RIE. Figure 1 shows Cr dots with 25 nm diam and 25 nm spacings on a bulk semiconductor substrate. In our experiment a variety of samples with different pitch size and areas were used for different purposes, as discussed later.

Chlorine-based RIE was used to transform sub-50 nm-diam Cr dot patterns into Si pillars. The etching was performed in a parallel plate RIE system operated at 13.56 MHz, with Cl_2 and $SiCl_4$ flow rates of 55 and 10 sccm, respectively, a power density of 0.32 W/cm^2, a pressure of 40 mTorr and a self-bias of −85 V. The etch rate of Si was 150 nm/min. The high selectivity of the chlorine RIE process is high, approximately 40:1 (Si/Cr), therefore insuring a minimal change in mask geometry during etching. Sub-50 nm diam pillars, 500 nm tall and with near vertical sidewalls, were routinely obtained. Figure 2 shows typical etched Si pillars with the chrome masks still in place. Such 3×3 arrays of pillars of a 150 nm period were patterned to calibrate the three steps of the pillar sculpting process. The chrome masks were later chemically removed using a wet etch (Cyantek Cr-7s).

The last step of the fabrication process utilizes aqueous HF acid etching (49%) to further reduce the size of the pillars and passivate the Si surface.[7]

III. FABRICATION RESULTS AND DISCUSSION

The effect of HF etching on pillar geometry was systematically studied. Figure 3 shows scanning electron micrographs of pillars at different stages of the etching process. Figure 3(a) shows a pillar just after RIE with the Cr mask still in place but before any HF etching. The pillar is approximately 45 nm in diameter and about 450 nm tall. The top of the pillar widens slightly due to sidewall deposition during RIE which has been observed before and can be

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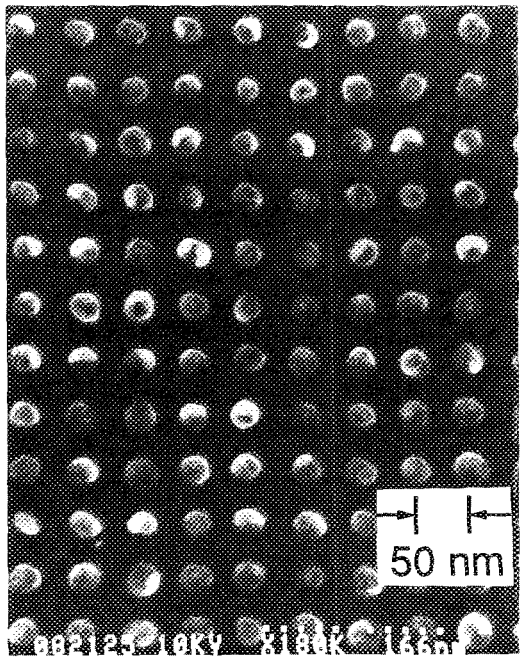

FIG. 1. Array of Ti/Au dots with 25 nm diam and 25 nm spacing on a bulk semiconductor substrate.

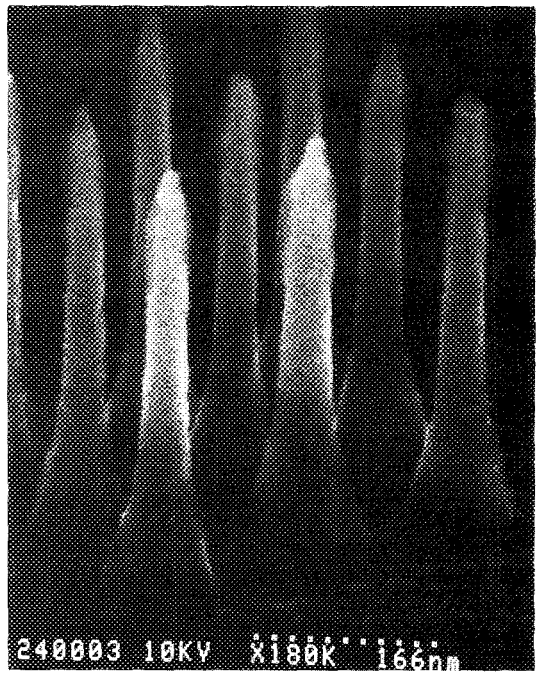

FIG. 2. Scanning electron micrograph of sub-50 nm diameter Si pillars with a period of 150 nm and a height of 500 nm.

readily removed by HF.[8] The bottom of the pillar widens out to form a pedestal due to the chosen RIE parameters. Figure 3(b) shows a pillar after removing the Cr and etching in HF for 4 h. The mushroom cap has been removed, resulting in a uniform Si pillar 25 nm in diameter. The overall height of this pillar is now about 350 nm. Figure 3(c) shows a pillar after a total of 8 h in HF. The pillar has been transformed into a nanoscale filament with a uniform diameter of about 10 nm and a length of 150 nm on top of a pedestal. The overall height is about 350 nm. It is possible to further reduce the size below 10 nm using this technique, but free standing Si pillars may become mechanically unstable at such small sizes. The array of pillars used for this study has an area of 34 μm$\times$26 μm and a period of 0.5 μm.

It should be pointed out that the pillars shown in Fig. 3 are different pillars from the same array to avoid problems caused by contamination during the SEM analysis. However, Fig. 3 should represent the actual evolution of a pillar during the processing, since the diameter of the pillars from the same array was found to be uniform. It should also be pointed out that during the high-resolution (ap-

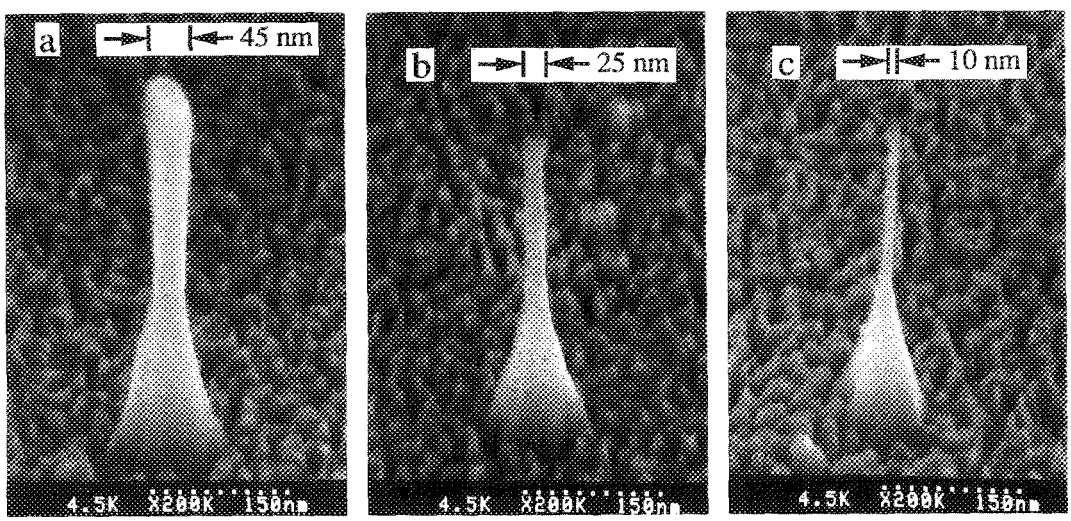

FIG. 3. Reduction of Si pillar diameters using HF etching: (a) No HF etching. The Cr mask is still in place. The pillar is 45 nm in diameter and 450 nm tall. (b) After removal of Cr and etching in HF for 3 h. The pillar is 25 nm in diameter and 350 nm tall. (c) After a total of 7 h in HF. The pillar is 10 nm in diameter and 350 nm tall. The top of the pillar is very uniform in width and has an aspect ratio in excess of 15.

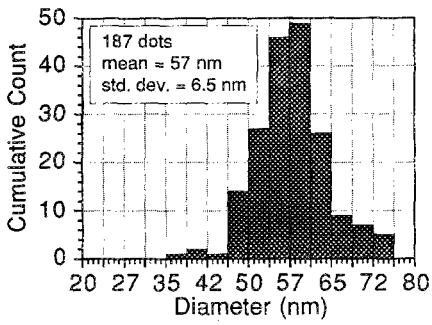

FIG. 4. Histogram of dot diameters from a 500 nm period test array.

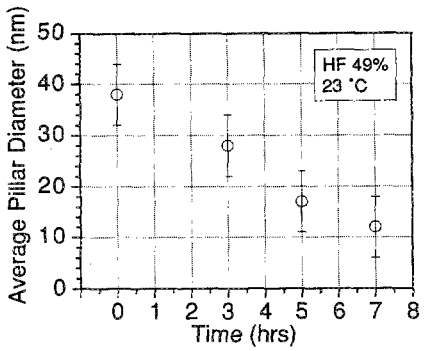

FIG. 5. Change in diameter with respect to time. The pillar diameters decrease at a rate of 3.8 nm/h. The error bars come from variations of the Cr masks.

proximately 3 nm), low voltage (<5 kV) SEM analysis no porous Si formations were observed.

The uniformity of this fabrication process was also studied. To determine the uniformity of the first step, the Cr mask definition, an array of Cr dots with a period of 500 nm was examined using an atomic force microscope (AFM). Such a large period was used to avoid the effects of the AFM tip size. A histogram of the dot diameters from a random sample of 187 dots (Fig. 4) shows that the average diameter of the dots is 57 nm with a standard deviation of 6.5 nm. The deviation in dot diameters most likely comes from noise in the beam deflection system. For the given exposure conditions, a beam deflection noise of 6.5 nm would translate to 3.6 mV of electronic noise. The pattern generator used for this project has a noise output of about 2 mV, and the SEM electronics could likely contribute an additional 1.6 mV of noise to the beam deflection signal. Another factor that might affect the variation in dot diameters is statistical variations of exposure dose, but this has been ruled out because the exposure dose is well above the threshold, and because of the relatively large number of electrons used at each point ($>6\times10^4$).

Proximity effects could also cause variations in dot diameters, but a detailed analysis indicates that the effect of proximity is rather negligible for the 500 nm period arrays exposed under the given conditions. However, proximity effects are not negligible for denser arrays. For example, to achieve the same dot diameter the required exposure dose in the center of a large area array of 150 nm period is 50% lower than that for a 500 nm period array. In the 150 nm period array, dots that are within the backscattered electron range (about 5–6 μm for the given conditions) from the edges of the exposure area will receive fewer backscattered electrons than those in the central region and hence have smaller diameters. This will tend to increase the variations of dot diameters. However, for an exposure area of 400×650 μm^2, 95% of the total exposure area is not affected by the edge effects and has uniform pillars diameters.

To determine the combined uniformity of the RIE and HF etching steps, a Si sample was patterned with arrays of Cr dots and etched using RIE and HF for 5 h. Subsequent high-resolution, low-voltage SEM measurements of 23 pillars determined that the standard deviation of pillar diameters was 5.7 nm. This deviation is very close to 6.5 nm—the standard deviation of the mask definition step—indicating that the RIE and HF processes are uniform and the definition of Cr masks is the factor limiting the uniformity of this process.

The silicon pillar etch rate in HF was calibrated using a high-resolution, low-voltage SEM before and at intervals after HF etching. To avoid complications of sample modification during SEM analysis, only virgin pillars were sampled at each time interval. It was found that HF etched Si pillar diameters at a constant rate of ~3.8 nm/h (corresponding to a single-sided etch rate of ~1.9 nm/h), as shown in Fig. 5. The results demonstrate that the HF etching process is very controllable. The error bars in Fig. 5 come from the variation of the Cr masks.

IV. PL MEASUREMENTS

PL measurements were performed at room temperature using an excitation wavelength of 532 nm from a Nd^{3+}:YAG laser. The beam was focused to a spot of about 100 μm diam and had a power density of 5 W/cm^2. The photoluminescence was analyzed using a 3/4 m monochrometer and was detected by a thermoelectrically cooled photomultiplier tube with a GaAs cathode. An initial sample had Si pillars with 50 nm diam, a period of 150 nm, and a length of 450 nm over an area of 600×450 μm^2. The pillar diameters were subsequently reduced using HF etching. PL measurements were done at various stages of the pillar diameter reduction process.

No PL was observed in the sample just after RIE or after removing the Cr and 4 h of HF etching. After 4 h of HF etching, SEM analysis found the pillar diameters to be 35 nm. After 8 h of HF etching, however, PL peaks centered at 720 nm were observed repeatedly from part of the pillar region but not from the bulk region of the same sample (Fig. 6). SEM analysis at this stage of the experiment found the pillar diameters to be about 20 nm. At this time, further analysis is needed to verify the origin of this PL.

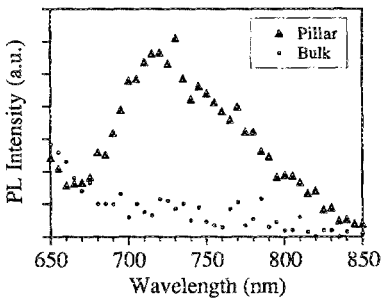

FIG. 6. The PL spectrum obtained from an array of nanoscale Si pillars. The PL peak is centered at 720 nm. The PL signal from the bulk was obtained from an unpatterned region near the pillar array.

V. CONCLUSIONS

A novel technique for fabricating free-standing Si pillars with diameters of about 10 nm and aspect ratios greater than 15 using EBL, RIE, and subsequent HF wet etching was presented. HF etching offers several advantages: it is a relatively stress independent process and therefore preserves the original shape of the structure; it is a room temperature process, making it a much more versatile process then high temperature oxidation; it has a very controllable etch rate (1.9 nm/h); and it can remove RIE damage and passivate the Si surface. The uniformity of this fabrication process was investigated. It was found that the standard deviation of pillar diameters can be controlled to within ± 6 nm and is limited by the etch mask definition. A PL peak centered at 720 nm was observed repeatedly from an array of nano-scale pillars. However, these results are preliminary and the cause of the PL is unclear.

ACKNOWLEDGMENTS

The authors would like to acknowledge fruitful discussions and assistance from Dr. Hans Lehmann, Dr. Edgar Steigmeier, and Dr. Nadim Maluf. We also thank Bob Guibord for providing assistance with electron beam lithography. The work was partly supported by a Packard Fellowship, SRC Contract No. 91-SJ-231, NSF, and AFOSR through an Air Force Laboratory Graduate Fellowship to P.B.F.

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