Steps and spikes in current-voltage characteristics of oxide/microcrystallite-silicon/oxide diodes

S. Y. Chou and A. E. Gordon
Department of Electrical Engineering, University of Minnesota, Minneapolis, Minnesota 55455

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SiO_2/microcrystallite-Si/SiO_2 diodes with different contact window sizes were fabricated and studied at room temperature, 77 K, and 4.2 K. Steps were observed in the current-voltage (I-V) characteristics at all three temperatures. These steps would appear for a certain number of measurements, depending upon measurement temperature, and then were replaced by a smooth electrical breakdown I-V characteristic. Data analysis indicates that the steps in the I-V characteristics are due to local electrical breakdowns along the edge of metal contacts instead of electron resonant tunneling through the structure. Surprisingly, however, in one diode, three repeatable spikes, instead of steps, were observed at 4.2 K; this cannot be satisfactorily explained in terms of electrical breakdown, and seems rather like electron resonant tunneling.

Excitement has been aroused by recent reports on room-temperature observation of negative differential conductances (NDCs) in a structure consisting of a 5 nm microcrystallite-silicon sandwiched between two 2-nm amorphous-Si_xC_{1-x}:H barriers,[1] and in a structure consisting of an 8-nm microcrystallite-silicon sandwiched between two 3-nm SiO_2 barriers.[2] These NDCs were attributed to electron resonant tunneling through microcrystallite (mc)-silicon, leading to a possibility that room-temperature quantum-effect devices could be realized in silicon—the backbone material of the integrated circuit industry.

In this letter, we present the study of diodes with a structure of SiO_2/mc-Si/SiO_2, similar to the one in Ref. 2, and report the observation of steps and spikes in the current-voltage (I-V) characteristics of these structures. We will show that the steps can be explained by local oxide breakdowns along the edge of the metal contact rather than electron resonant tunneling. However, the spikes in the I-V characteristics cannot be interpreted satisfactorily using the breakdown model.

In fabrication of SiO_2/mc-Si/SiO_2 diodes, 100-nm thermal oxide was first grown, using a wet oxidation and N_2 annealing, on an n-type silicon substrate with a phosphorus doping concentration of 8×10^{15} cm^{-3}. Then, the SiO_2 on the backside of the wafer was etched away and the backside was doped with phosphorous to form a $n+$ layer for a good back contact. Windows with different areas were opened in SiO_2 on the front side using HF etching, followed by a depositing of 12-nm-thick polysilicon using an electron-beam evaporation, with a substrate temperature of $\sim$60 °C at a pressure of 2×10^{-7} Torr. The polysilicon was then annealed and oxidized at 800 °C for 20 min in N_2/O_2 (with a 3:1 ratio) at atmosphere pressure. Due to fast diffusion of oxygen along the grain boundary, it is believed that, after the oxidation, the mc-Si becomes embodied into SiO_2. Comparing our fabrication process with literature[3] and extrapolating the anneal time, we estimate the mc-Si to have an average thickness of $\sim$9 nm and each oxide layer to have an average thickness of $\sim$4 nm. Literature[4] also indicates that the majority of these mc-Si should be in ⟨111⟩ orientation. Finally, the aluminum (Al) gate and Al substrate contacts (after etching away SiO_2 on the wafer backside) were deposited using electron-beam evaporation. The resulting structure is shown in Fig. 1.

Seven sizes of devices were fabricated on the same substrate, all of them squares, with sides of 4, 5, 8, 12.5, 37.5, 65, and 87 μm. An HP-4145B semiconductor analyzer was used in all measurements. The 77 and 4.2 K measurements were carried out by immersing the bonded devices in liquid nitrogen and liquid helium, respectively.

The I-V characteristics of a typical SiO_2/mc-Si/SiO_2 diode under forward bias conditions (i.e., the Al gate is positive) are very similar to a Schottky diode with an ideality factor of 11, 50, and 4000 at room temperature, 77 K, and 4.2 K, respectively.

Under a reverse bias and at room temperature, steps were observed in the I-V characteristics during the first measurement of the diodes (Fig. 2, curve a). In subsequent measurements, the steps disappeared and a smooth breakdown diode I-V characteristic resulted (Fig. 2, curve b). At 77 K, we found that the steps existed in three consecutive measurements before a breakdown I-V appeared and that, in the repeated measurements, each step generally did not occur at the same voltage as the previous measurement; they seemed rather random. At 4.2 K, the number of measurements that the steps exist increased to about ten before a breakdown diode I-V characteristic appeared. The steps at all three temperatures looked similar.

To study the origins of the stairs in I-V characteristics,

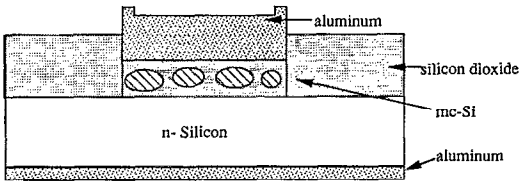

FIG. 1. Schematics of the cross section of an SiO_2/microcrystallite-Si/SiO_2 diode. The mc-Si has an average diameter of $\sim$9 nm and is sandwiched between $\sim$4 nm SiO_2.

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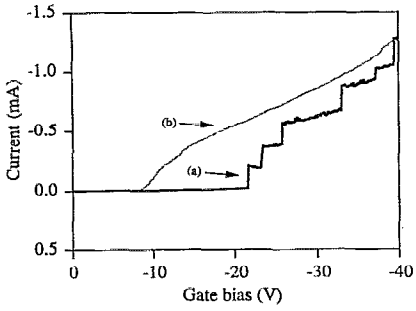

FIG. 2. Room-temperature current-voltage curve of a SiO_2/microcrystallite-Si/SiO_2 diode under a reverse bias. Curve a is the first measurement and curve b is the second measurement.

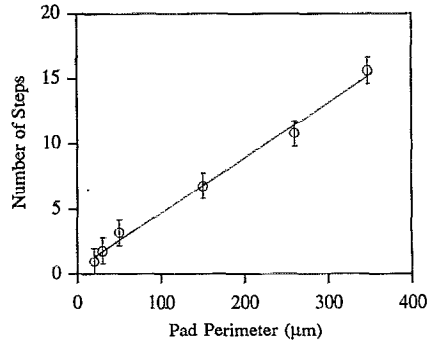

FIG. 4. Number of step vs perimeter of the contact window.

we conducted the following data analysis. First, we made a distribution of step height, and found that the distribution is independent of device area and measurement temperature. A typical step-height distribution is shown in Fig. 3. The average step height is $\sim 180\ \mu$A. If a step was due to tunneling through a silicon microcrystal, with a cross section of 9 by 9 nm^2, then the current density would have been 2×10^8 A/cm^2, which is so large that the Si microcrystal would have been melted immediately. Second, we plotted the current of the same diode in Fig. 2 (curve a) as a function of $1/V$. It showed that at low reverse bias, the diode current is logrithmically proportional to the inverse of the gate voltage, indicating Fowler and Nordheim tunneling, and at high reverse bias, the current increases very quickly with the gate voltage, indicating an impact ionization before the steps occur. Third, we plotted the number of steps versus the perimeter size of the contact window (Fig. 4) and found that they are proportional. Similar behavior was observed at 77 and 4.2 K. To determine the error bars, 50 devices were measured for each perimeter size. Fourth, we plotted the diode current after it had broken down (i.e., curve b in Fig. 2) at a given voltage versus the perimeter of the contact window and found that it is also proportional to the perimeter (Fig. 5). In other words, the breakdown current per unit perimeter size versus voltage characteristics are in fact independent of the contact-window size, indicating the breakdown current flow through the edge of the gate metal contact. And finally, if the steps were due to tunneling, their position should have been very reproducible, instead of random.

All of the above five observations indicate that a step in the I-V characteristic is not due to electron resonant tunneling but rather to a local electrical breakdown between the Si substrate and a point somewhere along the edge of the gate metal-contact pad. The sharp edge of a metal contact has a smaller radius of curvature, and therefore a higher electrical field. As a result, it is easier to electrically break down. Some studies showed that sharp edges in the metal contact can lower the oxide breakdown voltage by one-half or two-thirds.[5] We believe that in our case the breakdown starts at the weakest point of the structure (most likely at the edge of the contact), progresses to the next weakest point, and so on; each breakdown forms a step in the diode I-V characteristics. At room temperature, the breakdown current melts the material at the breakdown point due to Joule heating, and therefore, the breakdown is irreversible. This explains why the staircase could be seen only once at the room-temperature I-V. Such irreversible melting breakdown (but not the staircase) has been observed in metal-oxide-semiconductor systems.[6] On the other hand, at 77 and 4.2 K, the substrate is cooled by surrounding liquid and current heating is much less. Because the cooling prevents immediate melting of materials, the breakdown is initially an avalanche process and reversible, leading to repeatable staircase I-V characteristics. Obviously, the lower the temperature, the better the cooling and the more repeatable the staircase I-V characteristic. This is exactly what has been observed in the experiments.

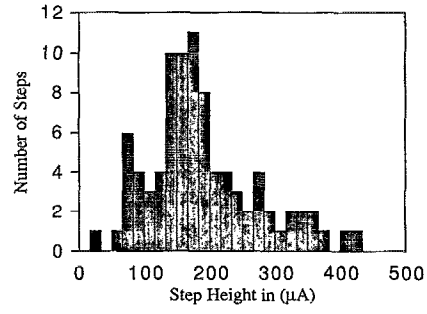

FIG. 3. Distribution of step height for an 87 by 87 μm^2 device at room temperature showing an average step height of 180 μA.

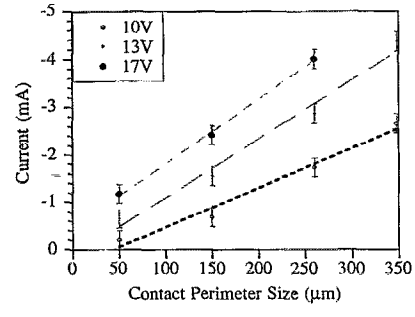

FIG. 5. The current in a diode already broken down at a fixed voltage vs perimeter of the contact window.

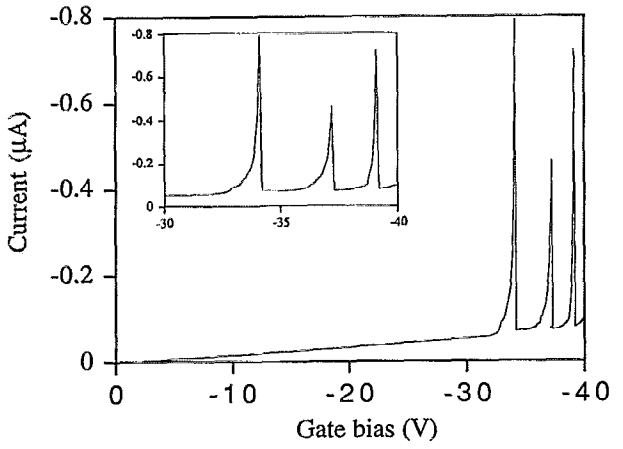

FIG. 6. The *I-V* characteristics of a SiO_2/microcrystallite-Si/SiO_2 diode of 4×4 μm^2 area at 4.2 K showing three repeatable spikes. The voltage increment during the measurements was 0.1 V.

To further prove that the steps in the diode *I-V* are due to electrical breakdown and that the breakdown causes material melting, we annealed the diodes that had broken down in a furnace at 150 °C for 1 h in the air and found that, after annealing, the staircase *I-V* characteristics reappeared. This is what we expected since annealing can oxidize the molten materials at the breakdown regions, making them insulators again.

One surprise appeared in our experiment, however: at 4.2 K, one of the devices with a cross section of 4×4 μm^2 fabricated on the same substrate showed three spikes in the *I-V* characteristic instead of steps (Fig. 6). We made six concurrent *I-V* measurements on the device before thermally recycling it, and the three peaks occurred at the same voltages as the previous measurements. The largest peak-to-valley current ratio of the spikes is 11. These spikes are difficult to understand in a local electrical-breakdown model. First, in the local electrical breakdown the voltage position for each breakdown should be random, but the three spikes occurred at the same voltages in every measurement. Second, the spikes go up gradually and smoothly instead of making large jumps as in the case of the staircase. Third, the current spike is about two orders of magnitude lower than the average step height (180 μA) for the staircase observed in other devices. If the current is due to tunneling through the Si microcrystal (9×9 nm),[2] the current density for each spike is about 1×10^6 A/cm^2, a reasonable number for tunneling. And finally, in the local electrical breakdown, the current step does not drop back but, in the spikes, the current does come back after the peak. We would say that the spikes in *I-V* characteristics look more like resonant tunneling than local electrical breakdown. The device was broken down when we thermally recycled it. More than 60 devices of the same cross section were measured at 4.2 K; none of them showed the spikes in the *I-V* characteristics. This makes it difficult to ascertain what caused the spikes; further investigation is in progress.

In summary, we have fabricated SiO_2/mc-Si/SiO_2 diode structures with different contact-window sizes. We have observed steps in the *I-V* characteristics at room temperature, 77 K, and 4.2 K. We have shown that these steps in the *I-V* are due to local electrical breakdowns instead of electron resonant tunneling. One device, however, showed three repeatable spikes in the *I-V* characteristics at 4.2 K, which resembles resonant tunneling rather than local electrical breakdown.

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