Multilevel nanoimprint lithography with submicron alignment over 4 in. Si wafers

Wei Zhang[a)] and Stephen Y. Chou
NanoStructure Laboratory, Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08544

We demonstrate that multilevel nanoimprint lithography (NIL) with submicron alignment over an entire 4 in. Si wafer can be achieved. Average alignment accuracy of 1 μm with a standard deviation 0.4 μm in both X and Y directions was obtained in ten consecutive tests of multilevel NIL. The multilevel alignment was achieved by aligning the wafer and the mask with an aligner, fixing them with a holder, and imprinting in an imprint machine. The issues that are critical to the alignment accuracy, such as relative movement during the press, relative thermal expansion, wafer bending, and resist, are discussed. The alignment accuracy currently achieved on the system is limited by the aligning accuracy of the aligner, instead of the process of multilevel NIL. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1391400]

Nanoimprint lithography (NIL)[1] has shown sub-10 nm resolution, high throughput, and low cost.[2] Single level NIL has been used to fabricate the critical patterns in many electronic and optical devices.[3–9] Several fabrication techniques,[10,11] imprint property of polymers,[12,13] and wafer scale imprint,[14,15] which make NIL more practical, have been studied.

For many applications, particularly integrated circuits, multilevel NIL with high overlay accuracy is essential. In this letter, we report an achievement of submicron alignment between two imprinted layers using a multilevel NIL system. We first discuss the issues related to achieving multilevel alignment of imprints, then describe our multilevel NIL system, and finally give the alignment results. Either thermal plastic polymer or curable polymer can be used as NIL resists. We used thermal plastic polymers as resist, which required heating and cooling during imprint.

To achieve the submicron alignment accuracy, we first studied a number of issues that can affect the alignment accuracy. The first issue is the relative mechanical shift between the mask and the substrate, which may occur when patterns on the mask are pressed into polymer resist. For a parallel plate imprint system, a large and uncontrollable relative shift and rotation between the mask and the substrate, shown by the misalignment map in Fig. 1, was observed after press by two parallel plates. Two reasons were considered to explain the relative shift and rotation between the mask and the substrate. (1) The two metal plates were not exactly parallel to each other due to the assembling tolerance and surface unflatness of the plates. (2) The rough surface of the metal plates applied nonuniform pressure on the mask and the substrate. To achieve high alignment accuracy, the relative shift between mask and substrate should be prevented during press. There are two approaches to solve the problem. One is to develop an imprint machine that does not cause the relative shift between mask and substrate during press. The other is to dynamically align the mask and the

substrate during press until the patterns on the mask are completely pressed into polymer resist.[16] We selected the first approach because we believed it had a higher throughput and could be easily combined with current alignment techniques and systems of photolithography.

Second, relative thermal expansion between the mask and wafer can cause misalignment when the mask and wafer are at different material. Since the alignment is done at room temperature and the imprint is at a higher temperature, initially aligned patterns can become misaligned during the imprint. For example, the thermal expansion coefficients of SiO_2 and Si, which are $5\times10^{-7}/°C$ and $2.6\times10^{-6}/°C$, respectively, give a relative thermal expansion coefficient difference $2.1\times10^{-6}/°C$. Assuming mask and wafer are aligned at $23\,°C$, and the centers remain aligned during press, the misalignment at the edge of the 4 in. Si wafer due to relative thermal expansion is about $100\,nm/°C$ increment. For imprints of using curable polymer as resist, the issue should also be paid attention to if the mask and wafer are heated during UV-cure exposure. To eliminate relative thermal expansion, we chose the mask material same as the wafer. In this case, 4 in. Si wafer was used as the substrate of the mask. Since the mask and wafer are made of the same
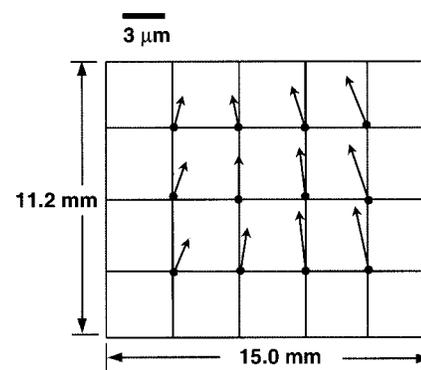

FIG. 1. The misalignment map showing relative shift and rotation between the mask and substrate during parallel plate imprint.

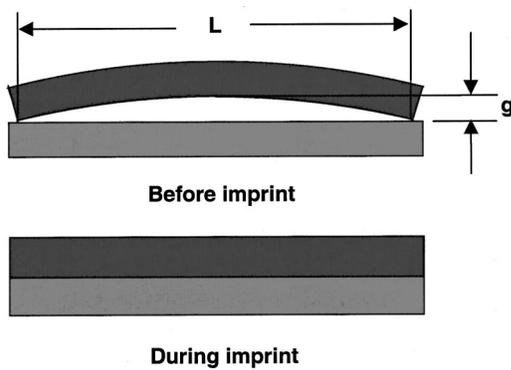[a)]Electronic mail: weizhang@ee.princeton.edu

FIG. 2. Estimation of misalignment due to bending wafers. Misalignment of wafer bending $\sigma = g^2/(6L)$, where g is a surface variation over an area with characteristic length L. Assume $g = 10 \ \mu m$, $L = 1$ cm for the worst case of Si wafer, $\sigma = 1.7$ nm.

material, there is not any relative thermal expansion as long as they are heated uniformly.

Third, wafer bending during imprint may result in misalignment. Because the mask and wafer surfaces are not absolutely flat, the mask and wafer will be bent to contact during the press, causing relative shift between the two patterns that are aligned before the press. In Fig. 2, we estimated misalignment of bending wafer by assuming a bow shape surface of the wafer. In the worst case, assuming $\pm 5 \ \mu m$ surface variation within an area about 1 cm wide, misalignment of bending wafer is on the order of nanometers. Thus misalignment due to bending wafers is not significant. In addition, we conclude that imprint pressure should be large enough to overcome the unflatness of mask and wafer.

Fourth, the resists that can be imprinted at lower temperature could improve alignment uniformity, because lower imprint temperature generally has better temperature uniformity control during imprint. To reduce resist surface variation over whole wafer after imprint, a customer-made resist (NP-33) with much better flowing than poly(methylmethacylate) (PMMA) is used in this study, which has an imprint temperature 100 °C and imprint pressure 100 psi. The temperature and pressure are much lower than 175 °C and 600 psi needed for 15 K PMMA resist.

Our multilevel NIL system consists of three parts: a commercial contact aligner, a wafer and mask transfer holder, and an imprint machine built in house [Fig. 3(a)]. At the beginning, mask and wafer are aligned and contacted on the aligner. Because both the mask and wafer are opaque, an image processing technique using visible light to align the mask and wafer, which aligns the align marks on back of the mask with the stored images of align marks on the wafer grabbed before by cameras of microscope, is used. Then, the mask and wafer are fixed by a holder and transported from the aligner to the imprint machine. The holder uses mechanical clamps to prevent relative movement between the mask and the wafer during transportation. Before the clamps are released and the holder is moved away, a prepress scheme is used to enhance friction force between the mask surface and the resist surface to prevent relative movement between the mask and the wafer due to vibrations that may occur during operation of the imprint machine. After the aligned set of the mask and wafer is taken off the holder and the holder is moved away, the aligned set of the mask and wafer is im-
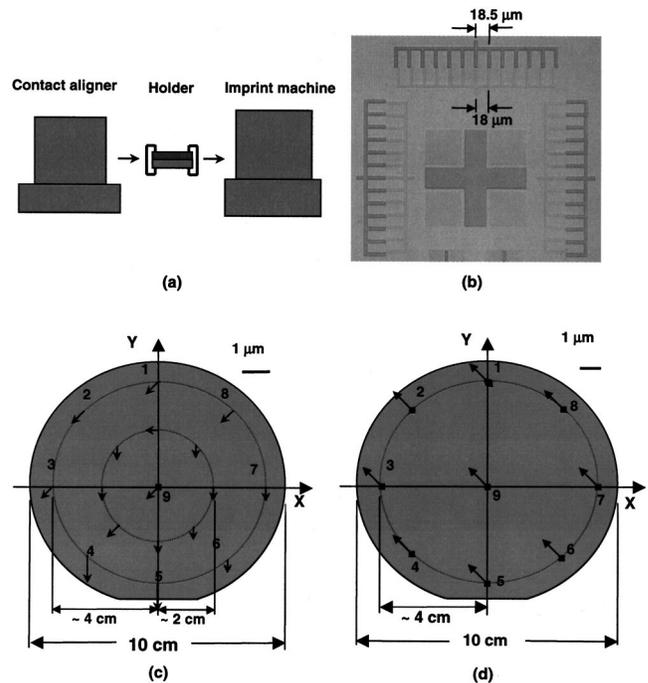

FIG. 3. The schematic of our multilevel NIL system (a), and the alignment results (b)–(d): (b) The image of alignment accuracy ($\Delta x = -0.5 \ \mu m$, $\Delta y = -0.5 \ \mu m$) of a typical multilevel NIL; (c) The global alignment map over 4 in. wafer of a run of multilevel NIL (average: $\Delta x = -0.3 \ \mu m$, $\Delta y = -0.5 \ \mu m$, standard deviation: $\sigma_x = 0.3 \ \mu m$, $\sigma_y = 0.2 \ \mu m$); (d) The global alignment map of a run without temperature nonuniformity during the imprint (center: $\Delta x = -1 \ \mu m$, $\Delta y = +1 \ \mu m$, average: $\Delta x = -1 \ \mu m$, $\Delta y = +1 \ \mu m$, standard deviation: $\sigma_x = 0 \ \mu m$, $\sigma_y = 0 \ \mu m$).

printed. After imprint, the subsequent processing is the same as single layer NIL without alignment. The imprint machine, which was developed in house (details will be published elsewhere), can simultaneously apply an uniform force over the entire mask and the wafer to eliminate relative shift and rotation.

A fabrication process, which involves the alignment of one imprint layer to a previous imprint layer, was used to demonstrate the multilevel NIL and its alignment accuracy. The first imprint level was a SiO_2 mesa fabricated by the first imprint, SiO_2 reactive ion etching (RIE) using the resist as the etching mask and removing the resist. After the wafer was cleaned by RCA No. 1 ($NH_4OH:H_2O_2:H_2O$ 1:1:5, 80 °C, 15 min), the second layer of resist patterns was imprinted by multilevel NIL with alignment to the first layer. The 4 in. Si masks used in imprints were fabricated by photolithography and SiO_2 etching (CHF_3 RIE) down to Si surface.

Submicron alignment of multilevel NIL over 4 in. Si wafer was achieved on the multilevel NIL system. The image of alignment accuracy of a typical multilevel NIL, which is at center of a wafer, is shown in Fig. 3(b). The faint color pattern is the SiO_2 layer fabricated by the first imprint and the dark color pattern is the second resist layer fabricated by multilevel NIL. The gratings of the two imprint layers, which have periods 18 and 18.5 μm, respectively, form an vernier that has measurement accuracy of misalignment 0.5 μm. The same vernier structure is also used as align marks to align the mask and wafer on the aligner. The global alignment map over 4 in. wafer of a run of multilevel NIL is given in Fig.

Data in X-direction: (μm)

Run #	1	2	3	4	5	6	7	8	9	Ave_s	σ_s
1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0
2	-1.5	-1	-2	-1	-1	-0.5	-0.5	-1	-1	-1	0.5
3	-1	-1	-1.5	-1.5	-1	-1	-1	-1	-1	-1	0.3
4	+0.5	+0.5	+0.5	+1	+1	+1	+1	+1	+0.5	+0.8	0.4
5	+2	+2	+2	+1	+1.5	+1	+1	+2	+1.5	+1.6	0.5
6	-0.5	-0.5	-1	-1	-1	-1	-0.5	-0.5	-0.7	-0.8	0.2
7	-2	-2	-2	-1	-1	-1	-1	-2	-1.5	-1.5	0.5
8	-2	-1.5	-0.5	0	+0.5	+0.5	-0.5	-1	-0.5	0.8	0.6
9	-1	-1	-1	-1	-0.5	-0.5	-0.5	-0.5	-1	-0.8	0.3
10	-0.5	-0.5	-0.5	0	0	0	0	-0.5	-0.5	-0.3	0.3
Ave_multi	1.2	1.1	1.2	0.9	0.9	0.8	0.7	1.1	0.9	1.0	
σ_multi	0.6	0.5	0.6	0.5	0.4	0.3	0.3	0.5	0.4	0.4	

Data in Y-direction: (μm)

Run #	1	2	3	4	5	6	7	8	9	Ave_s	σ_s
1	+1	+1	+1	+1	+1	+1	+1	+1	+1	+1	0
2	-1	-0.5	-1.5	-2	-1.5	-1	-1.5	-1	-1	-1	0.3
3	-1	-1.5	-2	-1.5	-1	-1	-1	-1	-1	-1.2	0.5
4	-0.5	-1	-1.5	-1.5	-1.5	0	0	0	-0.5	-0.7	0.6
5	+2	+2	+2	+2	+2	+1.5	+1	+1.5	+2	+1.8	0.4
6	-0.5	-0.5	0	0	-0.5	-1	-1	-1	-0.5	0.6	0.4
7	+0.5	0	-1	-1	0	0	+1	+1	0	0.5*	0.5
8	+1.5	+1	+0.5	+0.5	+1	+1.5	+2	+2	+1.5	1.3*	0.5
9	-2	-1.5	-1	-1.5	-2	-2	-2	-2	-1.5	-1.7	0.3
10	-0.5	-0.5	-0.5	-1	-1	-0.5	-0.5	-0.5	-0.5	-0.6	0.2
Ave_multi	1.1	1.0	1.1	1.2	1.2	1.0	1.1	1.1	1.0	1.0	
σ_multi	0.5	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.4	

FIG. 4. The alignment data and statistical average of ten consecutive runs of multilevel NIL. Note: The absolute values of data are used to calculate statistical average. The + or − sign is given to the average only when all data have the same + or − sign. * indicates runs that had inconsistent signs in their alignment data.

3(c), where the arrows represent direction and amplitude of misalignments. Over the whole 4 in. wafer, alignment accuracy is within 1 μm in both X and Y directions. The average of all locations in the alignment map gives −0.3 μm in the X direction with a standard deviation 0.3 μm and −0.5 μm in the Y direction with a standard deviation 0.2 μm, in which the values smaller than 0.5 μm means they are below the measurement accuracy of 0.5 μm. During imprint, temperature nonuniformity, which is the temperature difference between the mask and the wafer on same location, will cause misalignment between the mask and wafer due to thermal expansion. From the global alignment map, we found there was temperature nonuniformity over 4 in. wafer during the imprint, which caused the nonuniform distribution of the alignment map. With improved temperature uniformity by reducing the power of heaters during the imprint in another run of multilevel NIL, an uniform global alignment map was obtained [Fig. 3(d)], which has very uniform 1 μm alignment accuracy in both X and Y directions over whole 4 in. wafer. The temperature uniformity control of imprint machine still needs to be improved. We found the global alignment distribution is determined by two factors, the alignment distribution achieved on aligner by the operator, and the temperature uniformity during the imprint.

Alignment results of ten consecutive runs are shown in Fig. 4. In the tables, each row corresponding to one of the ten multilevel NIL runs gives alignment accuracy at the nine locations over 4 in. wafer shown in Fig. 3(d). The columns of Ave_s and σ_s give statistical average and standard deviation of alignments of nine locations for each single run. The rows of Ave_multi and σ_multi give statistical average and standard deviation of alignments on same location of the ten runs. The total average of the all ten runs is 1.0 μm in both X and Y directions with a standard deviation 0.4 μm. From the alignment averages of each single run in the tables, the probability to get average alignment accuracy within 1 μm (≤ 1 μm) is 80% in the X direction and 60% in the Y direction. The difference of probability between the X and Y directions is due to statistical variation.

The intrinsic machine resolution of the aligner in our multilevel NIL system is 0.5 μm, and the alignment accuracy that can be reliably achieved in aligning the mask and wafer on the aligner is 1 μm. So, the alignment accuracy of multilevel NIL currently achieved on the system is limited by the aligner other than the process of multilevel NIL.

In summary, we report the development of multilevel NIL and demonstrate sub-micron alignment over 4 in. Si wafers by multilevel NIL. The system and its process are fully scalable for 6 in. or larger wafer processing. Device applications of multilevel NIL are in progress.

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