Multi-Channel DVB-T Transmitter Design

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Abstract. This paper presents DTV transmitter design based on the SW/HW hybrid architecture. Parts of the DTV transmission algorithm with less computational complexity are processed by the SW module in PC whereas computationally intensive parts are processed by the HW module in FPGA. The two parts are interconnected by the high speed serial link. To provide the multi-channel DTV signal, we design an architecture where several DTV waveforms are generated simultaneously and combined in the digital domain. We propose a simulink based communication system design and verification and methodology. This method reduces the design and verification time of the prototype system significantly and reduces the RTL coding and verification burden.

Keywords: DTV transmitter, DVB-T, Simulink, FPGA, Multi-channel.

1 Introduction

Recently new DTV technologies have been developed to improve the mobile reception performance and also to provide high data throughput, including standards such as an ATSC 8VSB/MH [1, 2] or DVB-T/T2 [3]. Furthermore more sophisticated transmission technology is being developed to make it feasible to enjoy the ultra high definition (UHDTV) theater-class picture quality at home. To consider these various DTV transmission technologies, we need a flexible architecture for the DTV transmitter/receiver design.

In this paper, we propose the Matlab simulink model based system design methodology to ease the RTL coding and reduce the system development/verification time. We first use the floating point Matlab simulator for the performance verification. Next we replace the floating point simulink block with fixed point Xilinx system generation block and generate the net list automatically without RTL coding. Finally we synthesize the circuit in FPGA with Xilinx ISE design suite. This methodology can reduce the development and verification time of the proposed system significantly.

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2 System Description

The block diagram of the proposed system is described in Fig. 1. Part of the DVB-T system which requires relatively small computation is processed by the SW subsystem in PC. The processed streams are delivered to the FPGA HW subsystem by the high speed serial link. The DVB-T block which requires high computation is processed by the FPGA subsystem. Finally the result is delivered to the RF module.

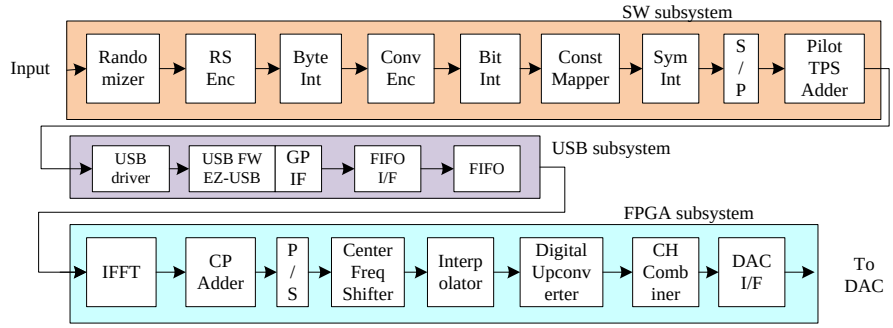

Fig. 1. DVB-T transmission system block diagram.

3 Design Methodology

To implement the multi-channel DTV transmitter, we propose a system level design methodology where we use the Matlab simulink with Xilinx block set tool box. The design process is described in Fig. 4. First we model the total transmitter system with Matlab script file and verify the system. Then we convert the double precision simulator to a fixed point simulator and trade-off between the performance loss due to the quantization effect and the system complexity. Next, we replace the fixed point simulink model block with Xilinx block to generate the net-list to be implemented in FPGA. By the design flow, we reduce the RTL coding and verification burden significantly since the EDIF net-list and the wrapper codes are generated automatically by the Matlab simulink without any RTL coding. We only need to implement the top level interface to integrate the wrapper code and some small logic blocks for the USB 2.0 and NAND flash memory interface. For the verification of the DVB-T transmitter, we also implemented the double precision DVB-T receiver with a sharp band-pass filter to select one of the 4 transmitted channel signal in Fig. 3. To avoid the performance loss due to the receiver processing, we use the same timing and carrier frequency information that is used in the transmitter. The BER (bit error rate) of the DVB-T receiver output is measured to confirm the transmitter performance.

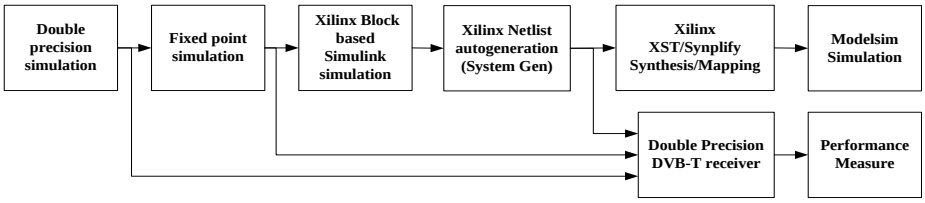

Fig. 2. Design flow of the DTV transmitter system using Matlab simulink and Xilinx block set.

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