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A CMOS 5th Elliptic Gm-C Filter Using a New Fully Differential Transconductor

Junho Bang, Jeho Song, Inho Ryu and Sunghaeng Jo

IT Applied System Engineering, Chonbuk National University, 567 Baekje-daero, deokjin-gu, Jeonju-si, Jeollabuk-do 561-756, Korea

Telephone: +82-63-270-4777, Fax: +82-63-270-4542, E-mail: songjh@jbnu.ac.kr

Abstract

A new fully differential transconductor for realization of CMOS analog Gm-C filter is presented. The presented transconductor offers the advantage of a high gain and small size. And the designed fully differential transconductor and a typical transconductor have been compared for a gain and frequency. In additional to as a application example a 5th Elliptic CMOS Gm-C using the proposed transconductors is designed. The results of HSPICE simulation using 1.8V-0.18㎛ CMOS processing parameter shows that the designed filter can be operated at supply voltage of 1.8V and the control range of the cutoff frequency is from 1.5㎒ to3.5㎒.

Keywords: *Fully differential transconductor, Gm-C filter, Continuous-time filter, Transconductor, Low-pass filter*

1. Introduction

The trend of development of analog signal processing filter chip has designers require high speed, high gain and low power consumption while it can be supplied by the low voltage. So many references have presented analog filters which can be operated at low supply voltage of 1V. And many design methodologies have been proposed to develop the low voltage filter [1-8]. In [3] among methods to design active filter, gyrator realization method that is simpler than other methods and uses transconductor in a more advantageous way for frequency characteristic is most widely used [4]. This method uses gyrator which is a bundle of transconductors and simulates inductor which is passive circuit. It is especially suitable for implementing active filters of bands from MHz to tens MHz. Also, it can materialize low voltage filters according to the designing method of transconductor in order to design low voltage signal processing filters. The structure of transconductor is in most cases similar to an operational amplifier except the structural difference of output impedance, so as to improve transconductor new methods have been developed in [9-16]. Ref. [9] utilized a CMOS self-bias differential amplifier in order to design a low-voltage transconductor. The CMOS self-bias differential amplifier has not only low voltage but also high speed performance like as references [10, 11, and 12]. So it has been used in high speed comparator for ADC and a low voltage current feedback amplifier. This circuit is operated by input signals without supply voltage from outside in accordance with self-bias characteristic, and it operates some transistors that form the amplifier in the linear regime and get the high speed performance. However, if this circuit is applied in an application field that needs more than 60dB profit, it requires additional connection for gain stage. Thus it results in a disadvantage that the

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frequency bandwidth of the circuit considerably decreases. So in an effort to improve such a disadvantage, in this paper the parallel connection method is suggested that it remains the strength of CMOS self-bias differential amplifier's low voltage and high speed increasing the profit as well as improves the frequency bandwidth. Through small-signal equivalent circuit analysis, it is proved that the parallel connection can improve the profit of circuit and the frequency bandwidth. Also, CMOS self-bias differential amplifier's phase reduction that was caused by the parallel connection structure is compensated with additionally formed compensating circuit. In Chapter 2, it examined the existing CMOS self-bias differential amplifier's characteristics and suggested ways to increase profits of amplifier through the parallel connection method. In Chapter 3, A CMOS 5th elliptic Gm-C filter using a new fully differential transconductor formed gyrators is designed and finally reached the conclusion in Chapter 4. All the circuits designed in this paper were simulated in HSPICE with CMOS 1.8V 0.8 ㎛ process parameter.

2. A New Fully Differential Transconductor

A new fully differential transconductor is newly designed as shown in Figure 1. The new fully differential transconductor utilizes the CMOS self-bias invertible differential amplifier [3] as a basic structure and completes its design in a parallel connection. As noticed in the circuit in Figure 1, the whole circuits are connected in a bilateral symmetry, the amplifier that consists of M1a~M6a on the left side and the amplifier that consists of M1b~M6b on the right side. Also, the input and output of these amplifiers are cross connected, and self-biases are connected with MC1 and MC2 each other. The MOSs formed in symmetry of the circuits *a* and *b* were designed in the same size. M1~M4 work in a saturation region while M5~M6 work in the linear region ($V_{DS}<V_{GS}-V_{TH}$). Such operation makes it possible for drain/source voltage V_{DS5}, V_{DS6} of M5 and M6 to be set up as a very low price. As a result, the voltage level of node ⓐ and ⓑ is close to the voltage of V_{DD} and V_{SS} each. Therefore, the supply voltage(V_{DD}-V_{SS}) needed for working the entire circuit is as much as the price of $V_{ⓐ}$-$V_{ⓑ}$, this voltage needs only the voltage for working M1 and M2 as well as M3 and M4 in a saturation region, so it is set up in about $2V_{DSAT}+V_{Signal}$ price.

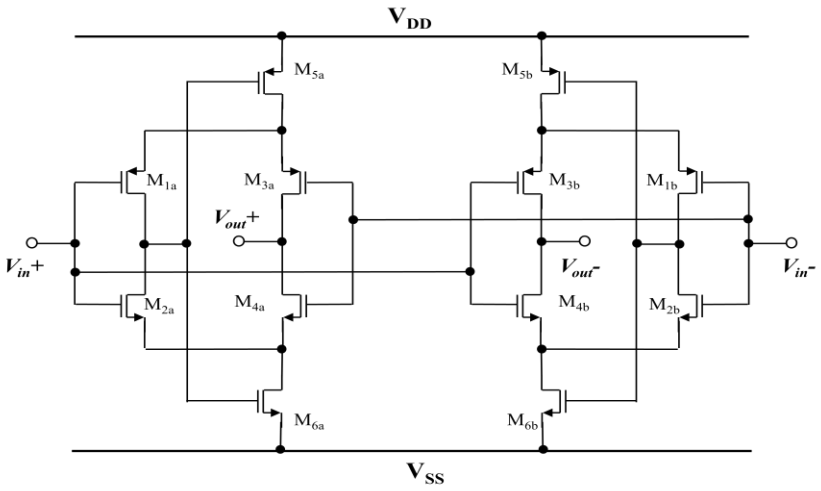


Figure 1. A new fully differential transconductor

To find the profit characteristics of CMOS self-bias differential amplifier in Figure 1, it is analyzed as shown by Figure 2 with small signal equivalent circuit. Figure 2 is only about a left part circuit and small signal equivalent circuit of Figure 1 and it is the same as the circuit in Reference [1]. If M1a, M3a and M2a, M4a are formed in a symmetry for each to have same sizes, current i_{d1} and i_{d2} that flow the differential circuit of both side will have the same size. When the small signal applies to it, currents are given by (1).

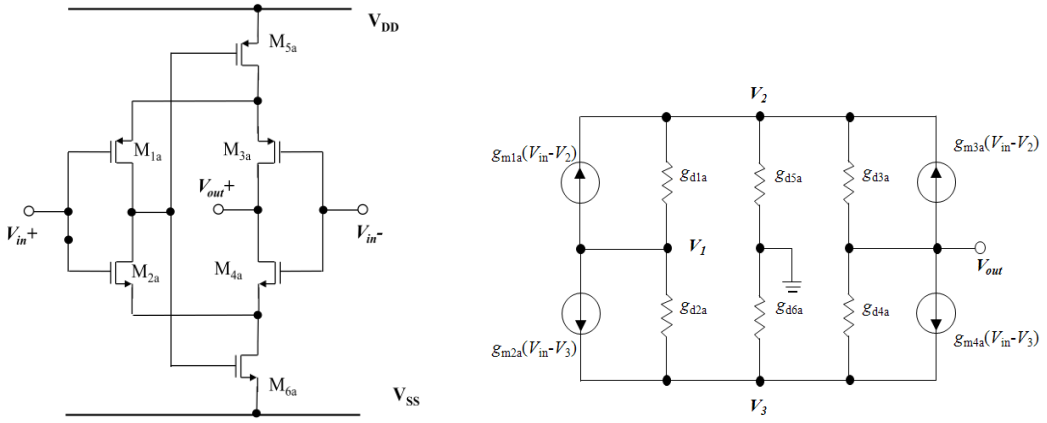


Figure 2. (a) Left side circuit of the fully differential transconductor, (b) Small signal equivalent circuit

$$i_{d1} + i_{d2} = 0 \tag{1}$$

At that point, i_{d1} and i_{d2} are becoming (2) each from small signal equivalent circuit in Figure 2(b),

$$i_{d1} \cong g_{m2}(\upsilon_{in1} - \upsilon_3) + g_{m1}(\upsilon_{in1} - \upsilon_2), \quad i_{d2} \cong g_{m4}(\upsilon_{in2} - \upsilon_3) + g_{m3}(\upsilon_{in2} - \upsilon_2) \tag{2}$$

the sum of these currents is (3).

$$i_{d1} + i_{d2} \cong g_{m2}(\upsilon_{in1} - \upsilon_3) + g_{m1}(\upsilon_{in1} - \upsilon_2) + g_{m4}(\upsilon_{in1} - \upsilon_3) + g_{m3}(\upsilon_{in2} - \upsilon_2) \cong 0 \tag{3}$$

In here, M1, M2 and M3, M4 each have different sizes and formed $g_{m1} \approx g_{m3}$, $g_{m2} \approx g_{m4}$ symmetrically. Also, if the terminal voltage v2 and v3 are designed in same size, it finally becomes like (4)

$$i_{d1} + i_{d2} \cong g_{m2}(\upsilon_{in1} - \upsilon_3) + g_{m1}(\upsilon_{in1} - \upsilon_3) + g_{m2}(\upsilon_{in2} - \upsilon_3) + g_{m1}(\upsilon_{in2} - \upsilon_3) \cong 0 \tag{4}$$

Here, $\upsilon_3 \cong \dfrac{\upsilon_{in1} + \upsilon_{in2}}{2}$ Therefore, i_{d1} is the same as (5).

$$i_{d1} \cong (g_{m1} + g_{m2})\upsilon_{in1} - (g_{m1} + g_{m2})\upsilon_3 \tag{5}$$

$$\cong (g_{m1}+g_{m2})\upsilon_{in1}-(g_{m1}+g_{m2})(\upsilon_{in1}+\upsilon_{in2})/2$$

$$\cong \frac{(g_{m1}+g_{m2})}{2}(\upsilon_{in1}-\upsilon_{in2}) \cong -i_{d2}$$

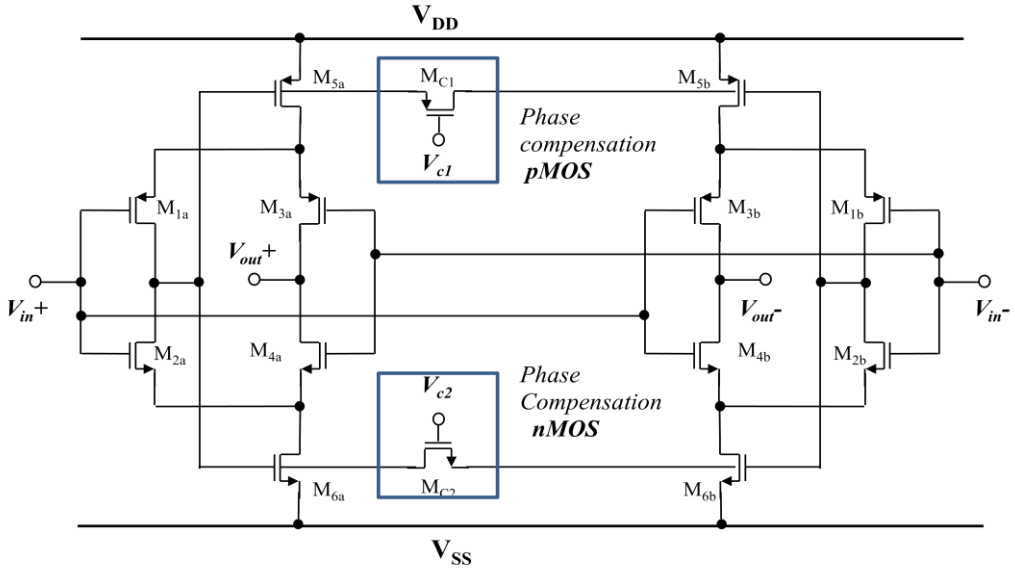
At this point, output resistance consists of M3 and M4's drain resistance, so the output voltage is like (6).

$$\upsilon_{out} \cong \frac{2i_{d1}}{(g_{m3}+g_{m4})} \cong \frac{(g_{m1}+g_{m2})(g_{in1}+g_{in2})}{(g_{d3}+g_{d4})} \tag{6}$$

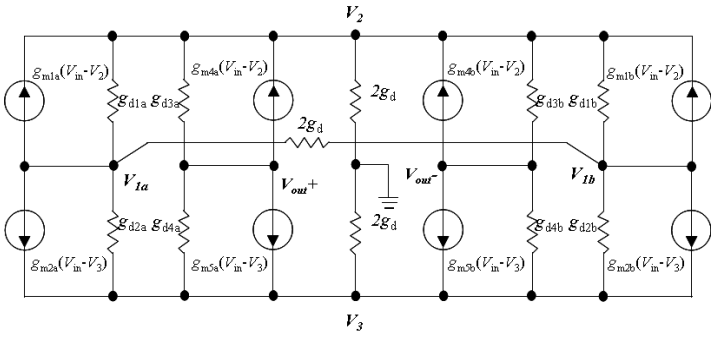
As a result, it reaches the conclusion that voltage profit of the left side circuit of the fully differential transconductor in Figure 1(a) is attained as it is shown in (7).

$$A_{dm} \cong \frac{\upsilon_{out}}{\upsilon_{in1}-\upsilon_{in2}} \cong \frac{(g_{in1}+g_{in2})}{(g_{d3}+g_{d4})} \tag{7}$$

As mentioned above, the left side circuit of the fully differential transconductor has an advantage of high speed performance. On the other hand, it is less profitable if it is applied in the filter and analogue-digital convertor by itself. In general, it requires 60dB of voltage gain to make it work as an operational amplifier and the left side circuit of the fully differential transconductor in Figure 2 gains only less than 60dB as it will be discussed in the latter part of this paper. Therefore, additional circuit is strongly required to increase the gain of the left side circuit of the fully differential transconductor. There are generally two methods to increase the gain of amplifiers: one is cascade gain stage connection [6] and the other is cascode connection [7] which increase gain by forming amplifying stage itself as a cascode. The cascade connection method is a method that can make high gain by subordinately connecting gain stages to differential amplifier stage. However, it has a major disadvantage that increasingly worsens frequency characteristic such as unity gain bandwidth as well as phasing characteristic so it requires additional compensating circuit. Moreover, the cascode connection method can pile up unit elements such MOS to differential amplifier and increase output resistance (R_o). Thus, it increases gain (A_v=g_m.R_o) price. But in this case, it needs an increase in supply voltage due to the elements added for consisting cascade. So, it is disadvantageous to use in low voltage circuit. Consequently, in this paper, it used parallel connection method for improving the gain of the fully differential transconductor and the whole structure of parallel type differential amplifier formed through this method shown in Figure 1 already. And the fully differential transconductor with MOSs (Mc1, Mc2) for compensating phase of the amplifier and the small signal equivalent circuit for analyzing the characteristic of this circuit are presented in Figure 3.



(a)



(b)

Figure 3. The new fully differential transconductor with MOSs (Mc1, Mc2) for compensating phase and the small signal equivalent circuit

The result of voltage gains that interpreted small signal circuits on the left and right side in Figure 3 are in (8) and (9).

$$A_{dm1} \cong \frac{\upsilon^{+}_{out}}{\upsilon_{in1} - \upsilon_{in2}} \cong \frac{(g_{m1a} + g_{m2a})}{(g_{d3a} + g_{d4a})} \tag{8}$$

$$A_{dm2} \cong \frac{\upsilon^{-}_{out}}{\upsilon_{in2} - \upsilon_{in1}} \cong \frac{(g_{m1b} + g_{m2b})}{(g_{d3b} + g_{d4b})} \tag{9}$$

According to (8) and (9), differential output about differential input is attained as it is found in (10).

$$A_{dm} \cong \frac{\upsilon^{+}_{out} - \upsilon^{-}_{out}}{\upsilon_{in1} - \upsilon_{in2}} \cong \frac{2(g_{m1} + g_{m2})}{(g_{d3} + g_{d4})} \tag{10}$$

Equation (10) shows how the gain can be twice bigger compared to the Equation (8) and (9) that consisted of one gain stage. This has been checked through HSPICE simulation and produced the characteristics as in Figure 4. In Figure 4, it proved that the proposed fully differential transconductor gained twice bigger gain (6dB) while the typical CMOS differential amplifier gained only 58dB of gain. Also, the frequency characteristic has improved as well that the proposed fully differential transconductor got 49MHz of frequency price which has increased from 20 MHz in the typical circuit to 29MHz.

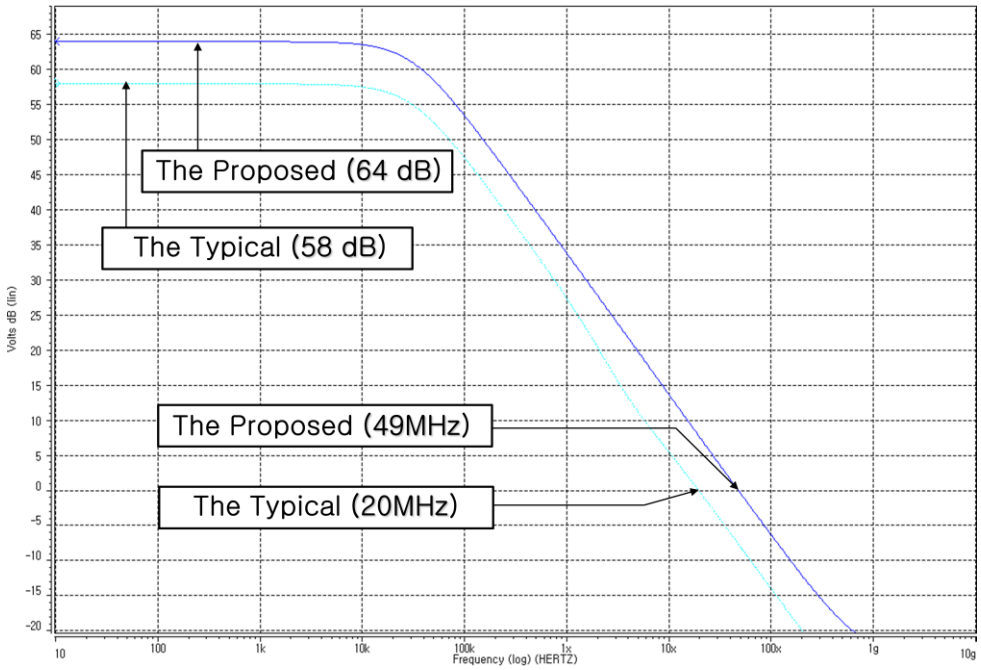


Figure 4. The gain and frequency characteristics of the proposed and typical transconductor

But the phase characteristic of the proposed fully differential transconductor ended up a bad result so the compensating circuit M_{c1} and M_{c2} have added to solve this. Figure 5 shows the phase characteristic of the proposed transconductor. The phase has fallen down to 60 degree in some frequency sections but the compensated phase rose up to more than 90 degrees in all bands within unit gain frequency.

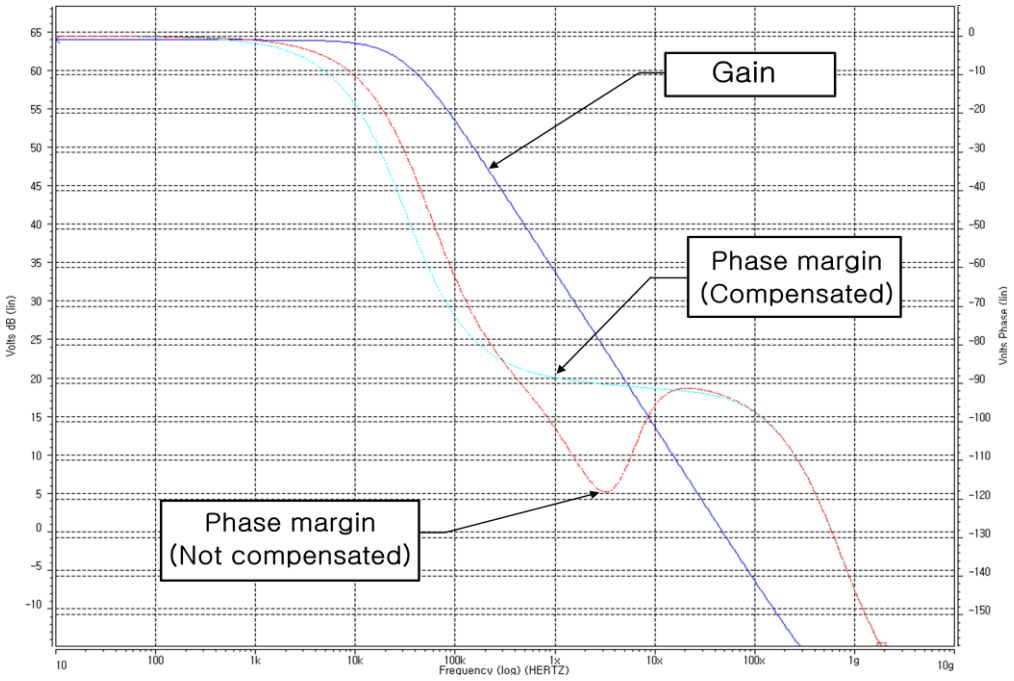


Figure 5. The compensated phase margin of the proposed transconductor

It did simulation on the whole characteristics of the proposed fully differential transconductor using standard 0.8 ㎛ CMOS process parameter and compared the typical circuit to the proposed differential transconductor [1] and arranged the result in Table 1.

Table 1. Comparison between the proposed and the typical fully differential transconductor

Design parameter	The typical transconductor	The proposed transconductor
Parameter	0.8 ㎛ CMOS	0.8 ㎛ CMOS
Supply voltage	1.8V	1.8V
Output load capacitor	1 pF	1 pF
Unity gain frequency	20 MHz	49 MHz
Open loop gain	58 dB	64 dB
Phase margin	60 °	93°
Power consumption	0.08 mW	0.16 mW

As a result of the simulation under loading condition such as 1.8V supply voltage and 1pF, the proposed differential transconductor increases a certain degree of power consumption compared to the typical one but it improves in every other aspects such as gain, frequency and phase characteristics.

3. Design of a 5th Elliptic Gm-C Filter using the New Fully Differential Transconductor

This chapter will consider the effort to design the cutoff frequency 1.5 MHz low-pass filter in a low voltage structure among the active filters that are widely used in analog signal processing. The specification is set up as lowpass that has 1.3~1.5MHz cutoff frequency for the use of mobile RFID reader IC in reference [2] and it is arranged in Table 2.

Table 2. The specification for designing a 5th Elliptic lowpass filter

Design parameter	Design method and target value
Filter function	5th Elliptic
Passive network	Ladder doubly-terminated LC circuitry
Cutoff frequency	1.3～1.5MHz (Tuning function)
Passband Ripple	1dB
Passband attenuation	6dB(Doubly-terminated characteristic)
Stopband attenuation	Over 50dB at 2.5MHz
Power supply voltage	3.3V
Power consumption	Below 3mW

For designing a filter that is suitable to the design specification in Table 2, in the first stage of passive filter design, doubly-terminated ladder passive filter is used as a fundamental passive circuit which maintains low reception characteristic. It is shown in Figure 6.

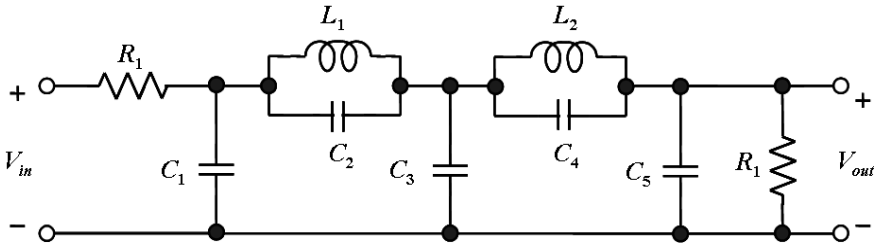


Figure 6. A 5th passive doubly-terminated ladder passive filter

Next is the converting step from a passive filter to an active filter. There are several passives to active conversion methods such as simulation method using gyrator, biquad method that connects second unit block to cascade form, and filter designing method using passive LC ladder type circuit to signal flow graph. But here gyrator direct converting method which is simpler to design is used. The designed 5th Gm-C active is shown in Figure 7.

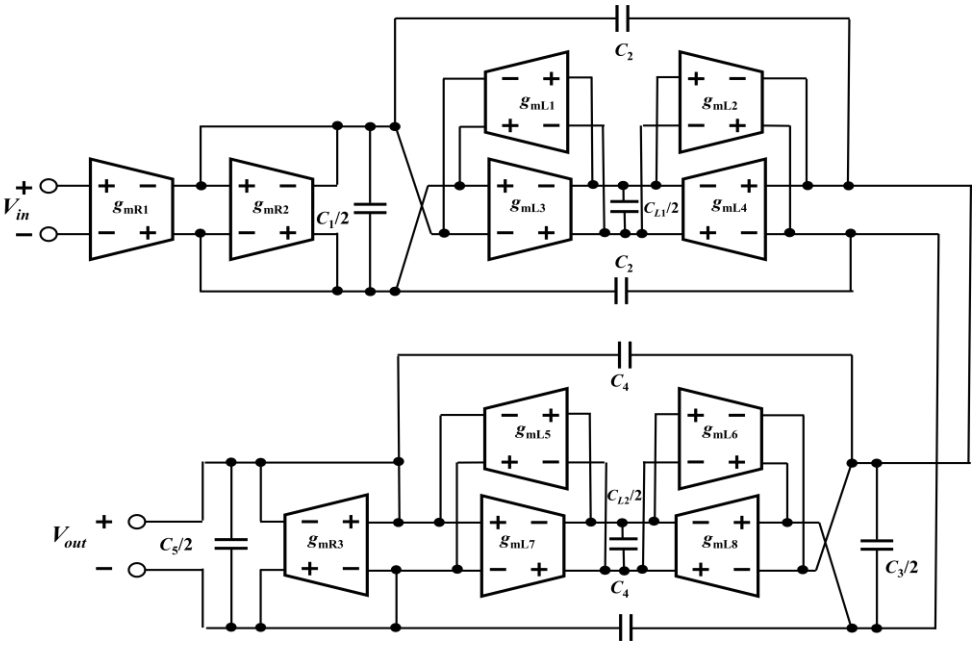


Figure 7. The designed 5th Gm-C active filter

The element 'L' of passive filter in Figure 6 is converted into active filter block which consists of four transconductors by gyrator direct converting method in Figure 7. Finally, the filter is completed connecting with the proposed fully differential transconductors in Figure 3, and the results of the simulation is shown in Figure 9.

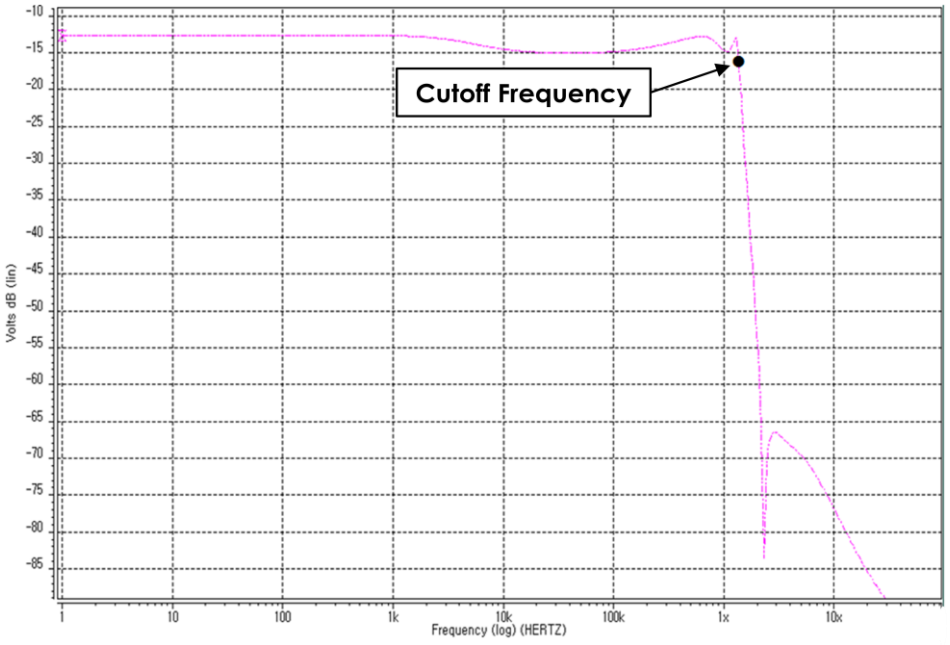


Figure 9. AC characteristics of the designed 5th Gm-C active filter

As Figure 9 shown, the filter's pass band showed gain attenuation feature of 12 dB higher than 6dB which is came up from the doubly terminated filter circuit. This can be compensated by adding gain compensating circuit when necessary. In the passing band, it provided damped oscillation ripple fit for the 5th elliptic filter feature. The cutoff frequency was 1.35MHz which satisfied the design specification of Table 1 that had been established before the drawing process. Over the attenuation of stop band, it had the value over 65dB at 2.5MHz, satisfying the design specification. The simulation result of entire electric power consumption got 1.9mW. This value was more superior low-power characteristic than the aimed design specification.

4. Conclusion

This paper present that the new fully differential transconductor is proposed to increase voltage gain of CMOS differential amplifier which was used in designing filter. As a result of the simulation, it has proved that the strength of the new fully differential transconductor is high speed performance and low voltage. And it is still maintained at the same time and it can increase the gain and frequency. The compared circuits are analyzed first in small signal equivalent circuit then simulated with CMOS 0.8 ㎛ process parameter HSPICE thus it had 64dB gain price which was increased twice more than the typical differential amplifier. Also, unit gain frequency in connection load capacitor as 1pF can be increased from 20MHz to 49MHz. Also, after forming with parallel connection method, in some frequency zones, phase characteristics fell down to nearly 60 degrees but two MOSs were used to form a compensating circuit in an effort of improving that problem. It resulted in a better phase characteristic which was restored up to 93 degrees even better than the existing phase. The filter for analog signal processing IC using the designed transconductor is designed and the simulation results show that it satisfied the design specification that cutoff frequency is 1.35MHz, low band reduction has the price of 2.5MHZ to 65dB. And also, it could gain 0.9mW of the entire power consumption which was better low power characteristics than expected.

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Authors

Jun-Ho Bang

He received the B.S., M.S. and ph. D Degrees in Department of Electric Engineering from ChonBuk National University in 1985 to 1996. He was senior researcher in the LG Semiconductor Institute of Technology from 1997 to 1998. He is currently a professor at Department of IT Applied System Engineering, ChonBuk National University since 1999. His research interests include integrated circuit design of the analog and digital mixed mode signal processing.

Je-Ho Song

He received the B.S. degree in Department of Electronic Engineering from Wonkwang University in 1991. He also received his M.S. degree in Department of Electronic Engineering from Wonkwang University in 1995, Ph.D. degree from Wonkwang University in 2003. He is currently a professor at Department of IT Applied System Engineering, ChonBuk National University since 1996. His research interests include VLSI, Information Communication, Communication Network System, and DSP design.

In-Ho Ryu

He received the B.S. degree in Department of Electric Engineering from Wonkwang University in 1984. He also received M.S Degree in Department of Electric Engineering from Konkuk University in 1986, Ph. D. Degree from Wonkwang University in 1993. He is currently a professor at Department of IT Applied System Engineering, ChonBuk National University since 1999. His research interests include FA system, Smart Grid and electric circuit system.

Sung-Haeng Jo

He received B.S. Degree in Department of IT Applied System from ChonBuk National University in 2013. He is currently a M.S. Degree course of IT Applied System from ChonBuk National University since 2013. His research interests include Integrated circuit design of system semiconductor.