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A 10 Gb/s Equalizer in 0.18μm CMOS Technology for High-speed SerDes

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Abstract. A 10 Gb/s equalizer consisting of analog equalizer and two-tap half-rate decision feedback equalizer (DFE) in a 0.18μm CMOS has been designer. By employing capacitive degeneration and inductive peaking techniques, the analog equalizer achieves large boosting. The pipelined half-rate architecture is used to improve the transmitted data rate in DFE with a small increase in area. Measurement results show that the distorted signal is well recovered by this equalizer and consumes 27 mW with the supply voltage of 1.8-V. The overall chip area including pads is 0.6×0.7 mm2.

Keyword: analog equalizer; decision feedback equalizer (DFE); capacitive degeneration; inductive peaking; current mode logic (CML)

1 Introduction

As wire-line communications systems continue to evolve to support ever-higher speeds, the channel inter-symbol interference (ISI) at high frequency is becoming more and more severe resulting in poor signal. There have been many reported methods to cancel the ISI. One of methods is using equalizer in receiver of systems. The equalizer in receiver can also be divided into two types: linear equalizer (LE) and decision feedback equalizer (DFE). LE can eliminate both pre-cursor and post-cursor ISI and is simpler in structure compared to DFE, but LE may increase noise and crosstalk. The DFE can eliminate post-cursor ISI without amplifying noise and crosstalk. However it may introduce the problem of error propagation [1-3]. From above viewpoint, this paper presents a 10 GB/s equalizer consisting of a linear equalizer and a nonlinear DFE in receiver for better equalization performance.

2 The Proposed Equalizer

In applications, there are also two typical linear equalizers: discrete-time FIR filter (FFE) and continuous time analog filter (analog equalizer). However, the implementation of FIR filter requires analog delay elements [3], which make them less practical, especially at higher data rates. On the other hand, alternatives to FIR filters include conventional high-frequency boost circuits that have a rational transfer

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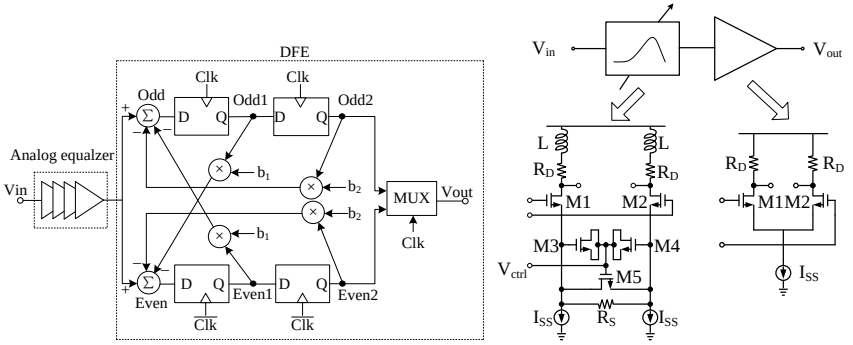
function [4]. The locations of poles and zeros could be adjusted to fit a desired transfer function to arbitrary accuracy. More important, the analog high-frequency boost circuit is employed in our design for its simplicity of implementation. Thus, this paper proposed is a 2-tap half-rate DFE combined with a analog equalizer in Fig.1 (a).



(a) (b)

Fig.1 (a) Block diagram of the proposed equalizer. (b)The circuit of analog equalizer

3 Circuit Design

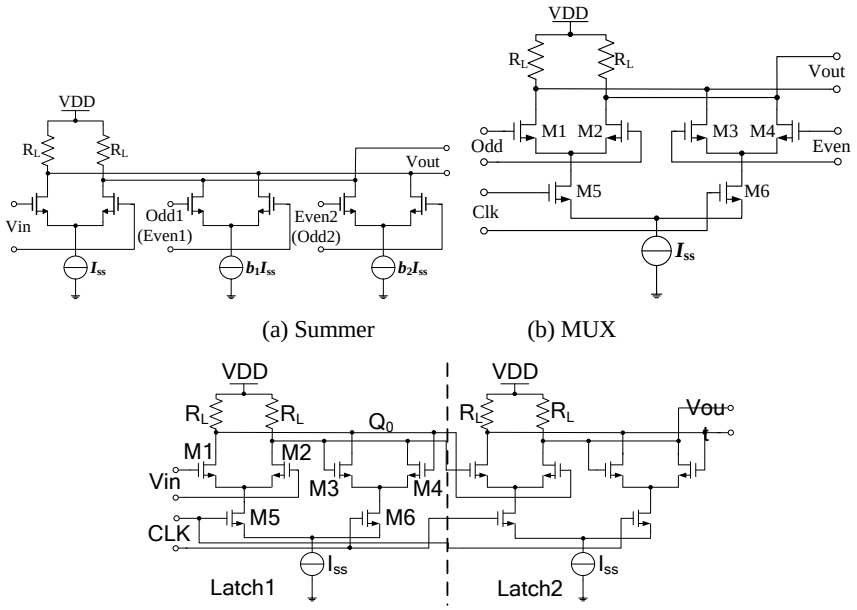
3.1 Analog equalizer

Shown in Fig.1 (b), the analog equalizer intersperses a peaking stages with a gain stages to provide a boost factor of about 10 dB at 10 GHz. The peaking stage in the equalizer path employs degeneration capacitance and inductive shunt peaking load to give a large boosting and high gain [5]. In the Figure, nMOS transistors M3 and M4 act as degeneration capacitance, nMOS transistors M5 acts as a variable degeneration resistance along with M3 and M4, where the boost range and the gain of the LE can be adjusted by changing the control voltage. As the control voltage rises, the on-resistance M5 of falls and so does the capacitance of M3 and M4, raising the magnitude of the zero.

3.2 Decision feedback equalizer (DFE)

A CML based summer, master-slave D flip-flop (MSDFF) and multiplexer (MUX) are employed in this DFE due to their advantage of high speed, shown as Fig.2. With the function of slicer and delay element in DFE, D flip-flop is one of the most critical components since it should work as fast as possible. The optimization of DFF is usually performed by reducing the sizes of the tracking transistors M1, M2, cross-coupled transistors M3, M4 and clock transistors M5, M6. The size, however, can not

be reduced too small. If it is reduced below a certain critical size, the cross-coupled pair will not latch. The sizes of tracking transistors M1, M2 and clock transistors M5, M6 are not also too small, since these differential pairs need to be large enough to switch the current correctly [6].



(a) Summer (b) MUX

(c) MSDFF

Fig.2 The CML-based circuit

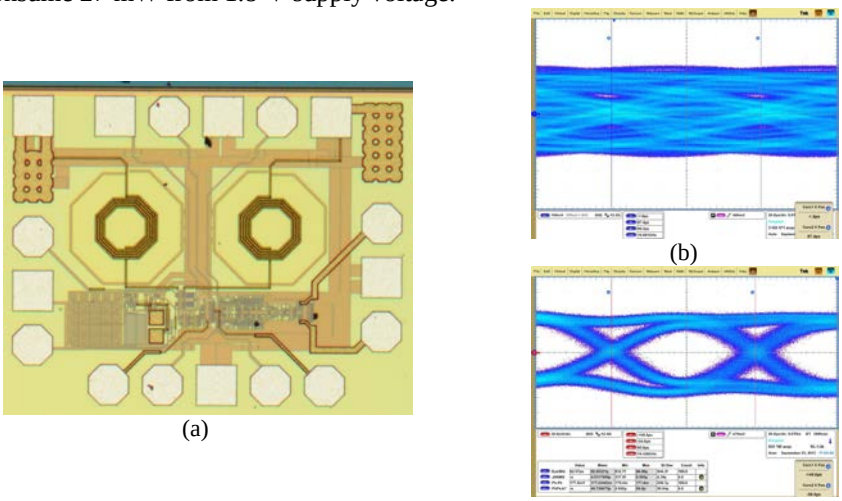
4 Measurement Results

The proposed equalizer has been designed and fabricated using 0.18μm CMOS technology. Fig. 3(a) shows the photograph of the equalizer. The overall chip area including pads is 0.6×0.7 mm^2. Fig.3(b), (c) gives the measured eye diagrams of 10 Gb/s PRBS data before and after the equalizer, respectively. From the figure, we can see that the majority of the ISI is removed, providing a horizontal eye opening of 0.62UI. This illustrates that the combined equalizer works well and is able to reduce ISI from the received data.

5 Conclusion

In this paper, a 10 Gb/s equalizer is realized in TSMC 0.18μm CMOS technology. The equalizer composed of an analog equalizer and 2-tap DFE enables error-free

NRZ signaling over a long backplane channel. Measurement results show that the equalizer chip can operate at data rates up to 10 Gb/s with an improved horizontal eye openings of 0.62 UI. The equalizer including pads occupies 0.6×0.7 mm2 and consume 27 mW from 1.8-V supply voltage.



(a) (b) (c)

Fig. 3 (a) Photomicrograph of the equalizer. (b) Measured eye diagram before equalization. (c) Measured eye diagram after equalization.

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