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Design of Fast Quantum-dot Cellular Automata Decoder

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Abstract. Decoders play an integral role in computer circuits. They are used in computer parts like random access memory(RAM). This paper presents a decoder with enable input. This decoder is developed using Quantum-dot cellular automata(QCA). QCA opens a completely radical way of microelectronics development and a potential replacement of CMOS based electronics. It ensures highly compact circuits, faster processing speeds, low power consumption. The use of clock in QCA provides power gain which is an important feature and this feature is not available in CMOS electronics.

Keywords: Quantum-dot cellular automata, Decoder, RAM.

1 Introduction

Continuous scaling down of CMOS technology is reaching its limiting levels. Further reduction in size has resulted in a number of problems for microelectronics although computing powers have increased at the same time. Some of the problems include interconnection of the circuit at such small scales and also high current leakage or inefficient power dissipation. All these problems require that an alternative technology be found that should replace CMOS technology. One such technology is quantum-dot cellular automata (QCA) [1, 2, 3].

QCA offers a number of advantages over CMOS technology. Some of the advantages include faster switching speeds, high density circuits and far less power dissipation. The assumption is that all these advantages will result in the development of highly powerful and efficient computers [4, 5].

2 Decoding Architecture

Decoders play an important role in computer architectures. They are used in different part of the computer like random access memory and they also form part of the look up Table (LUT) [6]. The decoder selects one out of several outputs lines when it has been activated for output. For the 3-input and 8-output decoder, one of the inputs is used to select the output [7].

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Table 1: The truth table of the decoder with enable (EN) line.

Input			Output			
A	B	EN	Y1	Y1	Y3	Y4
0	0	0	0	0	0	0
0	1	0	0	0	0	0
1	0	0	0	0	0	0
1	1	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

Several studies have been done on decoders in QCA. In [8], they proposed a 2 to 4 decoder using a 5-input majority gate. In this method, they reduced the number of gates to only four. This resulted in reduced delay and complexity of the decoder.

In [9], they proposed a 2 to 4 decoder. This decoder uses 4 majority gates in its structure and also uses 7 clock phases. This was extended to build a 3 to 8 decoder by using two 2 to 4 decoders. The 3 to 8 decoder uses a total of 8 majority gates and 11 clock phases.

3 Proposed Decoder

We propose a QCA decoder shown in Fig. 6. This decoder is made up of four 5-input majority gates. The gates were implemented as AND gates. As [8] pointed out, using traditional design methods will require a total of 8 gates. This will increase the complexity of the design as well as increase the delay time. The use of the four 5-input majority gate will result in the reduction in complexity of the circuit.

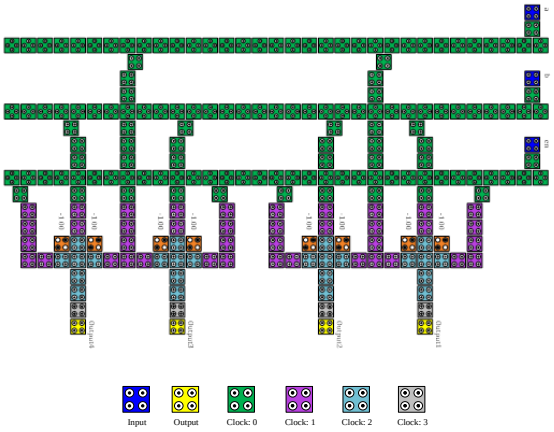

Fig. 6: Proposed structure of the QCA decoder.

This circuit was designed with the aim of reducing the delay time and thereby increasing the computational speeds. Therefore in this design we used only four clocks i.e. clock 1 to clock 3 as depicted by Fig. 6. In this circuit, we only used one layer (not multilayer) hence the use of the inverter chains with rotated cells to help in the signal to propagate properly.

4 Conclusions

In this paper, we have proposed a decoder that has a number of advantages. The first advantage is the reduced delay time. Our circuit delay time is only four clock phases i.e. only one clock cycle. This makes our circuit ideal to connect to other larger circuits or circuits where reduction in time will result in faster computation speeds. This will help in reducing the total delay time of those other circuits that will use our circuit as part of it.

In this paper we have also shown that, our proposed circuit has less number of cells as opposed to the circuit we compared with. This reduces the area that the circuit covers and this helps to reduce the overall area that the circuit covers when connected to other larger circuits.

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