AD-Census Based Real-Time Stereo Matching Hardware Architecture

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Abstract. In this paper, we propose a new stereo matching hardware architecture based on the AD-Census that produces accurate disparity map. The proposed architecture is fully pipelined and processes images with disparity level parallelism. The architecture is perfectly synchronized with the input camera clock for real-time performance. Its maximum clock frequency is 197 MHz when it is implemented in an FPGA device.

Keywords: AD-Census, Stereo matching, Disparity map, Real-time.

1 Introduction

Stereo matching is one of the most actively studied problems in computer vision. Most stereo matching algorithms can be classified into “global” and “local” methods. The global methods minimize energy function with dynamic programming [1], graph cuts [2] or belief propagation [3]. The global methods can successfully suppress the matching ambiguities caused by illumination variation and textureless regions. Thus, these methods generate more accurate results than local methods. However, they require high computational power for optimization process. The local methods compute each pixel’s disparity independently of the relationship with neighbor pixels and matching costs are extracted by simple measures such as absolute difference (AD), gradient and Census. The disparity level of each pixel is selected by minimal matching cost. Compared with global methods, the local methods are simpler and have relatively little computation time but they produce less accurate disparity maps.

In this paper, we aim to meet accurate stereo matching requirements with real-time performance by adopting the AD-Census stereo matching algorithm [4] and fully pipelined hardware architecture. The AD-Census algorithm has the combined features of AD and Census transform for more accurate stereo matching.

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The rest of the paper is organized as follows. In Section 2, we describe the proposed AD-Census hardware architecture. Section 3 presents the experimental environments, and then analyzes the results of the experiments. Finally, we summarize and conclude the paper in Section 4.

2 Proposed Hardware Architecture

Fig. 1 shows the proposed AD-Census hardware architecture. It aims at processing depth maps, synchronized with the input camera clock. For this reason, disparity level parallel processing is essentially required. The proposed AD-Census hardware architecture consists of the Image Memory, the Window Selector, the AD, the Census and the Depth Computation.

The Image Memory stores the left and right image data from the stereo camera line by line, and it outputs the line image data of the window region. The Window Selector aligns line image data depending on the window region. Each of the AD and Census compute the matching cost for depth computation using its own measure. The Depth Computation computes final matching cost and outputs the depth results by selecting minimum matching cost.

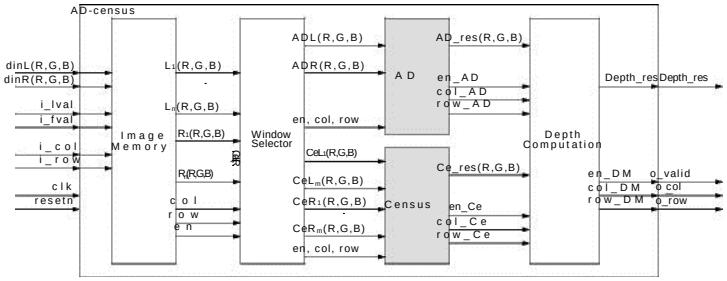


Fig. 1. Proposed AD-Census hardware architecture.

The AD cores for red, green and blue images have the same structure. Fig. 2 shows the AD core for red image processing. The Window Register_R has as many registers as the size of disparity range for disparity level parallelism. The Diff computes absolute difference between left and right pixels. The AD Cost computes the matching cost by summation of the absolute differences from the Diff.

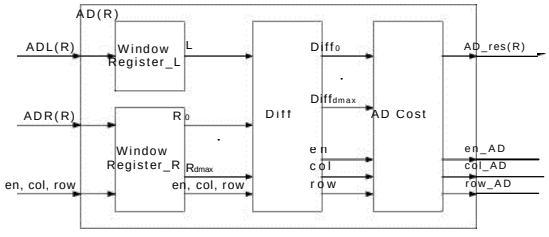


Fig. 2. Proposed AD core hardware architecture for red image.

The Census cores for red, green and blue images have the same structure like the AD cores. Fig. 3 shows the Census core for red image processing. The HW_comp makes the hamming weight bit stream through pixel comparison among the window regions. Also, the Census cores each have as many right hamming weight registers as the size of the disparity range like the AD cores. The Counter computes hamming distance by bitwise XOR operation between left and right hamming weights and outputs the hamming distances as Census matching costs.

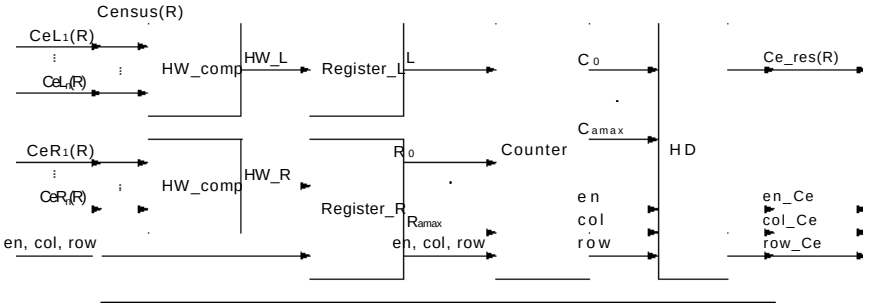


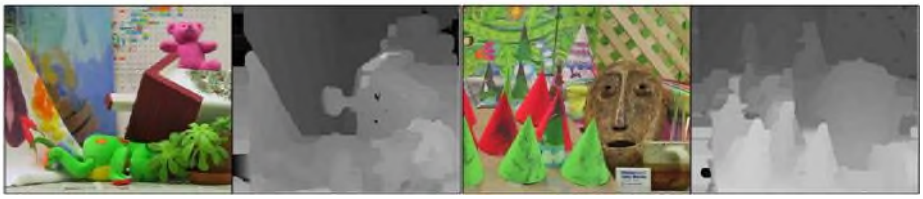
Fig. 3. Proposed Census core hardware architecture for red image.

3 Experimental Results

The proposed AD-Census hardware architecture is designed with an HDL and implemented in Xilinx Virtex6 LX760 FPGA. The proposed architecture has 64 disparity ranges. This architecture is compared with the hardware architecture of [5]. Table 1 shows the FPGA implementation result. Fig. 4 shows the results of AD-Census. As shown in the Fig. 4, the depth map is finely extracted. Even though the proposed hardware architecture is implemented by combining the AD and Census transform, the hardware usage is similar to that of [5] only with Census transform except for Slice LUTs. The proposed architecture is synchronized with the input camera clock with the maximum clock frequency of 197 MHz.

Table 1. FPGA Implementation Results.

	FPGA results		Characters
[5]	Slice Registers	53,616	Census transform
	Slice LUTs	60,598	Disparity range 64
	Block Ram/FIFO	192	Rectification included
Proposed	Slice Registers	67,650	AD-Census(AD + Census)
	Slice LUTs	126,850	Disparity range 64
	Block Ram/FIFO	32	



(a) Teddy image (b) Corn image

Fig. 4. Disparity map results of test images.

4 Conclusion

This paper proposes a new real-time stereo matching hardware architecture for the high performance and more accurate results. We adopt the AD-Census stereo matching algorithm which can reduce the matching errors caused at individual measures and produce accurate disparity map. The proposed AD-Census architecture is fully pipelined for real-time performance and its operation is synchronized with the input camera clock. It computes accurate disparity of each pixel with disparity level parallelism. According to the experimental results, the hardware usage of the proposed AD-Census hardware architecture is similar to that of [5] only with Census transform except for Slice LUTs. The maximum clock frequency of the proposed hardware architecture is 197 MHz in an implementation with an FPGA device, so it is able to support most existing cameras in real time.

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