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Improvement of Quantum-Dot Cellular Automata Decoder Using Inverter Chain

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Abstract. In this paper, we propose a combinational circuit such as decoder using quantum-dot cellular automata. Our circuit reduces both a delay time and a cell space, and it has also regular clock zones. The proposed scheme uses an inverter chain instead of inverter gates in order to minimize an area and time complexity. Our architecture has easy scalability and extension of circuits.

Keywords: Quantum-dot Cellular Automata, Decoder, Inverter Chain

1 Introduction

Nowadays a number of research on Quantum-dot Cellular Automata(QCA) decoders and their implementation in circuits have been done. In [1], they implemented a 2:4 decoder using a five-input majority gate with the aim of simplifying the structure. In this architecture particular emphasis was placed on the circuit stability. The 2:4 decoder that was presented in [2] uses three majority gates, two inverters and a coupled majority minority gate that outputs a majority and minority result simultaneously.

2 Quantum-Dot Cellular Automata

The basic building block of QCA is a cell. The cell is made up of 4 dots and two electrons. The electrons can tunnel around the cell but they cannot tunnel outside the cell. These electrons repel each other due to Coulombic interaction and occupy two opposite sites. This gives the cells stable states.

In QCA wires can also be formed by arranging cells one after the other in line. In the wire signals propagate from the input to the output and the cells will assume polarization of the input signal. An inverter chain is formed by aligning the quantum

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dots to be at 45 degree. The value in an inverter chain changes from ‘1’ to ‘0’ and vice versa as it moves along the wire. An inverter gate inverts an input (i.e. ‘1’ to ‘0’ and vice versa) as it moves in the gate. Lastly, a majority voting gate outputs the majority of the three input values [3].

Using the majority gate an AND gate and an OR can be implemented [3]. In QCA the flow and direction of information is controlled by the clock signal. In total there are four clock phases which are shifted by 90 degrees from the previous clock phase [4][5].

2 Proposed Scheme

A decoder is a device that selects one out of several output lines when activated for output. Most decoders have *n*-inputs and 2^n outputs. Some decoders have enable signal that selects the output line [6].

Our structure uses four majority gates and an inverter chain. Due to the behavior of the inverter chain the purely inverter gates were not used. The outputs for the decoder were placed outside of the main circuits to allow easy scalability and extension of the circuit.

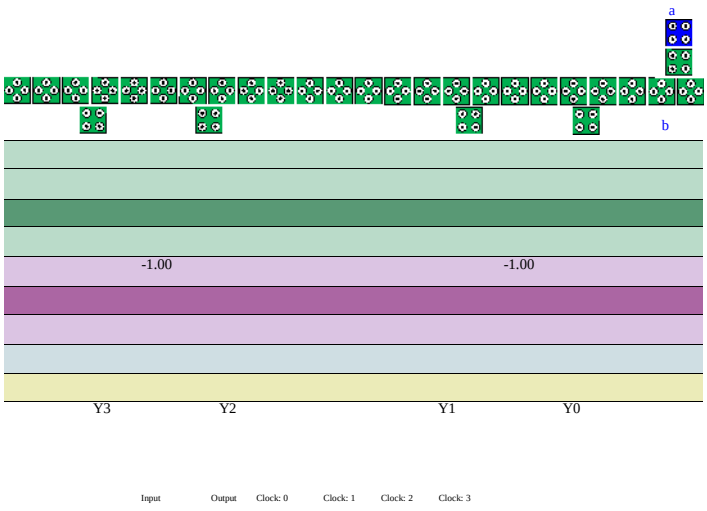

Fig.1. proposed combinational circuit using inverter chains

The simulation of the circuits was done using QCADesigner tool [7]. In QCADesigner, cells are assumed to have width and height of 18nm. The quantum-dots are also assumed to be 5nm in diameter and the cells are placed on a grid with center-to-center distance of 20nm [8].

The proposed designs were compared with the proposal in [2]. The main advantages of the proposed structure are that it has a fewer number of cells which results in reduced area and hence occupying a small area on the circuit.

The simulation results show that the outputs are produced after three clock phases which is an improvement on [2]. Table 1 gives the comparison between the circuits.

Table 1. Comparison of the properties between circuits.

	Proposed in [2]	Fig. 1
Number of cells	139	110
Area covered (nm^2)	163,592	129,624
Number of gates	6	4
Number of clock phases	5	3

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