Implementation of CMOS Receiver Front-End for WLAN/MAN

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Abstract. This paper describes a CMOS direct-conversion receiver front-end for 5GHz wireless LAN/MAN. Sub-harmonic mixing is used for down-conversion to minimize the DC-offset due to LO-leakage. To minimize the DC-offset due to LO self-mixing, sub-harmonic mixing is used for down-conversion. For quadrature down-conversion with sub-harmonic mixing, octa-phase LO signals are generated by octa-phase shifting network. Implemented in a 0.18μm CMOS technology, the receiver dissipates 62mA from a 1.8V supply voltage and has 3.1dB noise figure (NF) and -13dBm input third-order intercept point (iIP3).

Keywords: CMOS (Complementary Metal Oxide Semiconductor), Receiver Front-End, Cascode LNA, Mixer

1 Introduction

Among various kinds of wireless communication systems, wireless LAN/MAN is most popular for short range communications due to its high data rate. For low cost and low power implementation of WLAN terminal, fully-integrated CMOS RF transceiver is required for which low-IF or zero-IF (direct-conversion) architecture is most suited because the number of external components is minimized [1-3]. The 5GHz WLAN/MAN standard, IEEE 802.11a, 802.16a, is employing OFDM where the first sub-carrier is not used and the channel bandwidth is wide [4]. Therefore, it is relatively immune to DC-offset and flicker noise and direct-conversion receiver architecture has been a popular choice [1-2].

In this paper, implemented in a 0.18um CMOS technology, a fully-integrated CMOS direct conversion receiver front-end is described for 5GHz WLAN/MAN applications.

The block diagram of the direct-conversion receiver for 5GH WLAN/MAN is shown in Fig. 1.1.

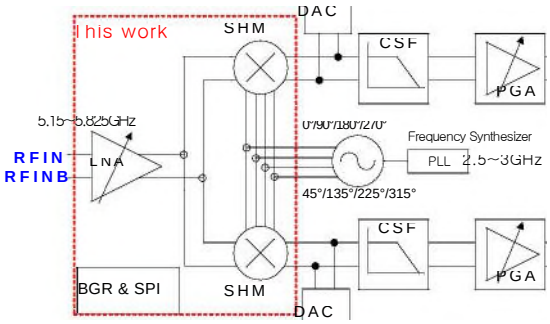

Fig. 1.1 Direct-conversion receiver for 5GHz WLAN/MAN.

2 Related study

2.1 LNA structure

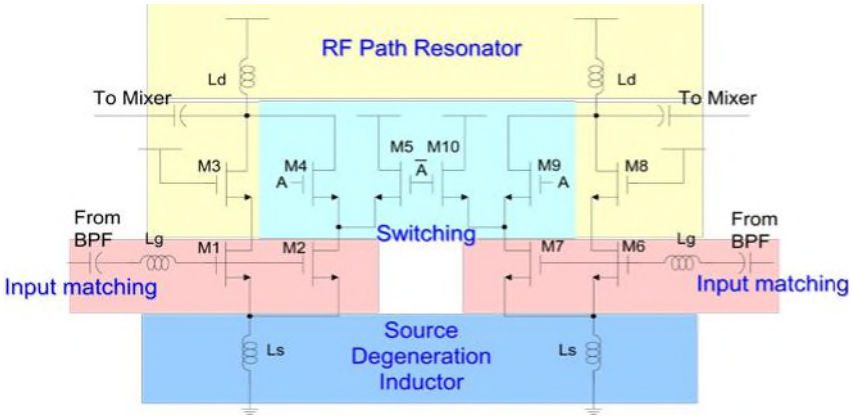

Fig. 2.1. The schematic of a LC-tuned pseudo differential LNA

The proposed schematic of a LC-tuned pseudo differential LNA is shown in Fig. 2.1. The LNA input is matched to the previous stage (e.g. output of an BPF). The LNA is based on the cascoded LNA structure with inductive degeneration and an inductive load. The pseudo differential low-noise amplifier uses the nMOS common-source cascode topology with inductive degeneration provided by bonding wire to minimize the chip size and to obtain a high Q-value. L_s is used source degeneration inductor and L_g is utilized with input impedance matching. The LNA has dual gain mode to relax the linearity requirement on down-conversion mixer. The LNA is switched to low gain mode to alleviate the linearity requirement on the following stages when large RF input signal is present. LC-tuned pseudo differential LNA is

used and two different voltage gain settings of 26 and 6dB can be selected by switching the input transconductance. In high-gain mode, all the signal currents are directed to the output load network. In low-gain mode, the signal current generated by the transistor M2 and M7 is directed to VDD. The degeneration inductor L_s is implemented using bonding wire.

2.2 Sub-harmonic Mixer structure

Fig. 2.2 shows a simplified schematic of a single-balanced mixer with inductive loads. With a high intermediate frequency, inductive loads can be used in place of resistive loads to improve the filtering of the LO feed-through while increasing the head-room of the circuit. The frequency of the LO is the half of the RF and therefore eight-phase LO signals spaced by 45^o are required for quadrature down-conversion. As shown in the figure, the I-mixer uses 0^o, 90^o, 180^o, and 270^o LO signals while for Q-channel, 45^o, 135^o, 225^o, and 315^o LO signals are used. The output of the transconductance stage is AC-coupled to the switching stage to prevent the low-frequency even-order harmonics and DC-offset of the transconductance stage from being leaked to the mixer output. Additional advantage of the AC-coupling is the independent biasing of the transconductance and switching stages, facilitating the design optimization such as the conversion gain, noise figure, and linearity. The output current of the mixer is converted to voltage by a first-order filter whose cutoff frequency is tuned by the same code as the channel selection filter following the mixer.

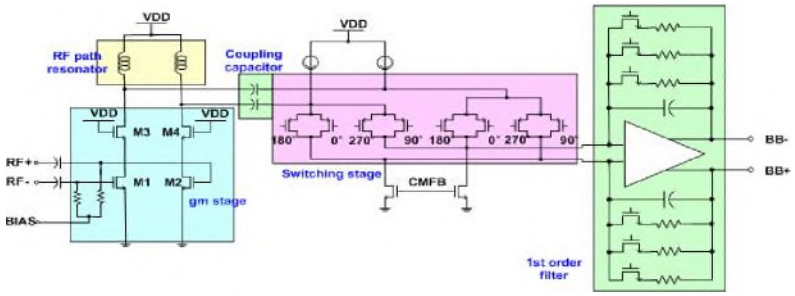

Fig. 2.2. Sub-harmonic mixer for I-channel

To minimize the noise contribution from the switching transistors, it is required to reduce the DC bias current of the switching stage and increase the LO amplitude as much as possible. In the proposed sub-harmonic mixer, the DC-bias of the switching stages is independent of the transconductance stage, allowing the simultaneously optimization of both the transconductance and switching stages. Moreover, the noise contribution of the switching stage is further reduced by resonating the parasitic capacitance at the node *A* with the inductors L_1 and L_2 [5].

3 An Experimental Result of WLAN/MAN Receiver Front-End

The WLAN/MAN receiver front-end has been implemented in 0.18um CMOS RF technology whose microphotograph is shown in Fig. 3.1. The chip occupies a core area of 2.1mm^2 and is packaged in a 48-pin MLF package with exposed die.
Measured voltage gain of the RF front-end is from 38.3dB to 38.7dB at high gain mode from 5.15 to 5.825GHz range as shown in Fig 3.2. Measured noise figure at LNA input is from 2.9dB to 3.1dB in the same frequency range as shown in Fig. 3.3. The third-order input intercept point (IIP3) of the RF front-end is measured to be -13dBm in LNA high-gain mode, as shown in Fig. 3.4 . The results of the linearity, noise figure and voltage gain simulation and measurement of RF front-end are summarized in Table. 3.1 with other performance parameters.

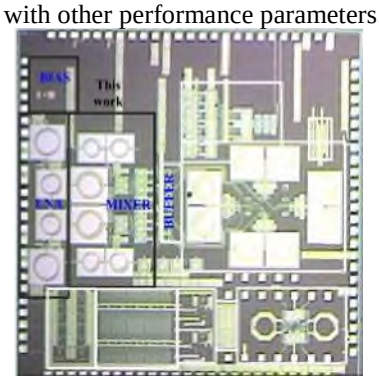

Fig. 3.1. Die microphotograph of the receiver Front-End

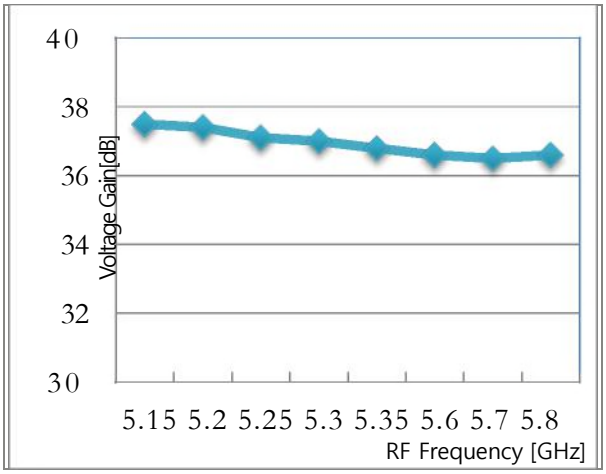

Fig. 3.2. Measurement of front-end voltage gain at high gain mode

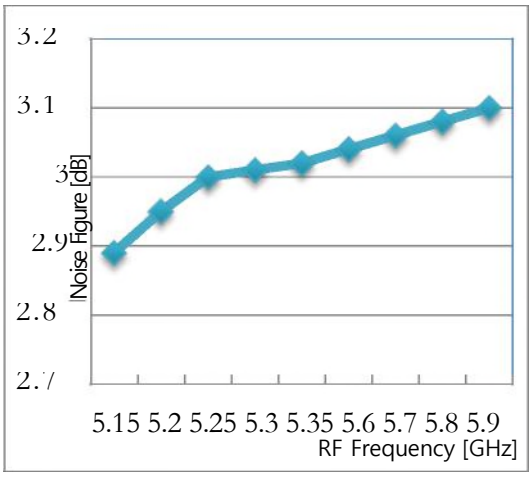

Fig. 3.3. Measured Noise Figure at high gain mode

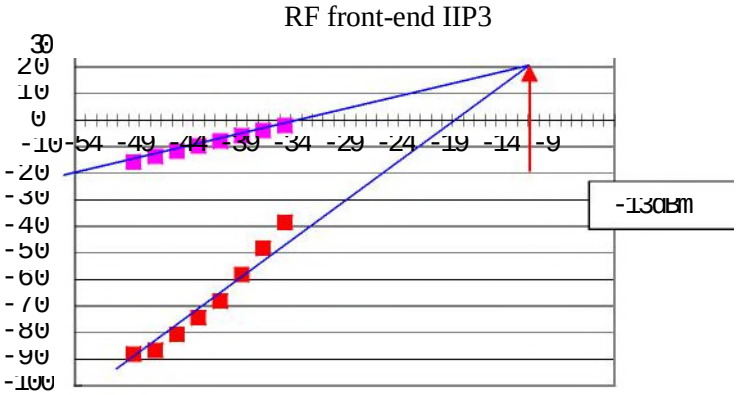

Fig. 3.4. Measured IIP3

Table 3.1. Measured performance of RF Front-end

Parameters	Spec.	Post simulation	Meas. Results
Frequency(GHz)	5.15~5.825	5.15~5.825	5.15~5.825
Voltage Gain[dB]	28~38	37.5	36.5~37.5
P1dB [dBm]	-22	-22	-21.4
iIP3 [dBm]	-15	-13.5	-13
Noise Figure[dB]	3.2	2.9	2.88~3.1
Power Cons.[mW]	65	62.4	62.4

4 Conclusion

This paper describes a CMOS direct-conversion receiver front-end for 5GHz wireless LAN/MAN. Sub-harmonic mixing is used for down-conversion to minimize the DC-offset due to LO-leakage. To minimize the DC-offset due to LO self-mixing, sub-harmonic mixing is used for down-conversion. For quadrature down-conversion with sub-harmonic mixing, octa-phase LO signals are generated by multi-phase shifting network. Implemented in a 0.18um CMOS technology, the receiver dissipates 62mA from a 1.8V supply voltage and has 3.1dB noise figure (NF) and -13dBm input third-order intercept point (iIP3).

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