NAND-block Level Buffer Replacement Considering Write Frequency

Ilhoon Shin

NowonGu GongleungDong, Seoul National University of Science and Technology,
Building 3,207, Seoul 139-743, South Korea
ilhoon.shin@snut.ac.kr

Abstract. NAND based block devices such as solid state drives have an internal RAM to maintain the mapping table between logical sectors and their physical location. The available space can be used as buffer to absorb read/write requests. This paper discusses an efficient buffer replacement policy on the internal RAM, which performs a block-level buffer replacement considering write frequency.

Keywords: Write frequency, LRU, Buffer replacement, NAND flash memory

1 Introduction

NAND flash memory has the strengths of light-weight, low energy consumption, small form factor, silence, shock-resistance, and good read performance, and thereby NAND-based block devices such as solid state drives (SSDs), memory cards, and USB memory are popular in various computing environments. However, the write amplication and the according slow write performance, which derives from an erase-before-write feature, has been a problem.

Thus, lots of researches have been doing to improve the write performance by designing an efficient internal firmware, and one approach is to use an internal RAM in NAND-based block devices as buffer to absorb a portion of read/write requests [16]. If the required data are found in buffer, we do not need to access NAND flash memory and thereby the performance of the NAND based block devices is improved.

In order to maximize the effect of buffer, increasing the hit ratio is important, similarly to the case of traditional buffer in PCs and servers. However, in the case of NAND-based block devices, generating NAND-friendly write pattern is also critical, because the performance of NAND flash memory is seriously influenced by the write pattern. Thus, we need to design a buffer replacement policy to deliver a good hit ratio while at the same time generating NAND-friendly write pattern.

In order to increase hit ratio, the re-reference probability should be considered, and it is generally known that the temporal locality exists and influences on the re-reference likelihood. Thus, the buffer replacement scheme should become a variant of LRU replacement scheme, which selects a victim buffer considering the temporal locality.

Meanwhile, NAND friendly write pattern is a sequential pattern whose request size is the same with a NAND block. Thus, the buffer replacement scheme should be a variant of NAND-block level replacement scheme. In this work, we present the policy that considers the above points.

2 The Presented Scheme

There are several block level LRU replacement schemes that consider both temporal locality and NAND-friendly write pattern [3-6]. However, they have their own weaknesses. For example, rarely access pages that belong to hot block are not replaced in BLRU [3-4], which causes a waste of buffer space. On the contrary, PLRU-BR [5] causes hot pages to be replaced because they belong to the same block with rarely accessed pages, which decreases hit ratio. BLRU-BR-2Q [6] does not replace the hot pages when evicting the rarely accessed block. However, the average write request size is smaller than the BLRU and the PLRU-BR schemes.

Thus, the presented scheme compromises the existing schemes, especially BLRU and PLRU-BR-2Q. It usually operates the BLRU scheme to generate NAND-friendly write pattern. In order to address the weakness of the BLRU scheme that the rarely accessed pages are not evicted, it infrequently selects a victim block which has the least recently accessed page, and the victim block except the hot pages is written to NAND flash memory. Consequently, it can solve the problem of the BLRU scheme without damaging its strength.

3 Conclusion

We discussed and presented a buffer replacement scheme for NAND-based block devices. It considers both temporal locality and NAND-friendly write pattern. In order to address the weaknesses of the existing scheme, it compromised the BLRU and the PLRU-BR-2Q schemes. It basically operated the BLRU scheme, and however it selected the victim block infrequently in the same way with the PLRU-BR-2Q scheme. The important thing is to determine the ratio of operating the PLRU-BR-2Q scheme. It is a tuning parameter that influences the performance. We need to study the influence of the ratio and find the optimal value in the future work.

Acknowledgments This work was supported by Seoul National University of Science and Technology.

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