Advanced Science and Technology Letters
Vol.48 (CIA 2014), pp.87-94
http://dx.doi.org/10.14257/astl.2014.48.16

Multilevel PWM Inverter Employing a Modified Half-bridge Configuration with a Single DC Voltage Source

Feel-soon Kang[1], and Won Seok Choi[2]

[1] Dept. of Electronics and Control Engineering, Hanbat National University, Daejeon, Korea
[2] Dept. of Electrical Engineering, Hanbat National University, Daejeon, Korea
feelsoon@hanbat.ac.kr

Abstract. It presents a five-level PWM inverter using an isolated Half-bridge circuit configuration. Compared with a conventional cascaded H-bridge multilevel inverter synthesizing five-level on output voltage wave, the proposed approach generates the same voltage levels using an isolated Half-bridge configuration adding a switching device and a diode. Hence, it can reduce the number of switching devices up to three resulted in reduction of switching loss and conduction loss. Additionally, it just employs a single dc voltage source whereas the conventional approach needs two independent dc voltage sources. Moreover, it improves reliability and stability by applying a transformer ensuring a galvanic isolation between a dc voltage source and the output. To verify the validity of the proposed multilevel inverter, we carry out a computer-aided simulation.

Keywords: Cascaded H-bridge multilevel inverter (CHM), Half-bridge, Pulse Width Modulation (PWM), Total Harmonic Distortion (THD), and Transformer.

1 Introduction

Recently, multilevel inverters are researched to apply various high-power and high-voltage applications. By synthesizing several dc voltages, it generates an output voltage close to a sinusoidal wave. Switching loss and voltage rating of a switching device can be reduced by increasing the number of output voltage levels, which ensures a high quality output voltage with low THD. Multilevel inverters are classified by three categories; diode-clamped, flying-capacitors, and cascaded H-bridge types. Among them, cascaded H-bridge multilevel inverter is well known as the most useful circuit topology to increase the number of output voltage levels in an efficient manner [1]-[3]. It also shows a good characteristic on modularization. However, it is not the best choice to increase the number of output voltage levels because it still suffers from the number of switching devices and independent dc voltage sources. To solve the problem, many researchers focus on developing effective circuit topologies, which can reduce the number of components even though increasing the number of output voltage levels [3]-[9]. In [3], it has introduced a modified H-bridge inverter, which is useful to reduce the number of switching devices by adding an upper switching device at series-connected capacitors. It is a good

ISSN: 2287-1233 ASTL

solution to save switching devices. However, it does not deal with voltage unbalancing between series-connected capacitors. In this paper, we propose a new multilevel circuit topology, which is suitable for reducing switching devices even though increasing the number of output voltage levels. First, we explain the circuit configuration with valuable merits. Second, we analyze operational modes in a theoretical manner. Finally, performance and validity of the proposed approach are verified by computer-aided simulations.

2 Proposed 5-level PWM inverter

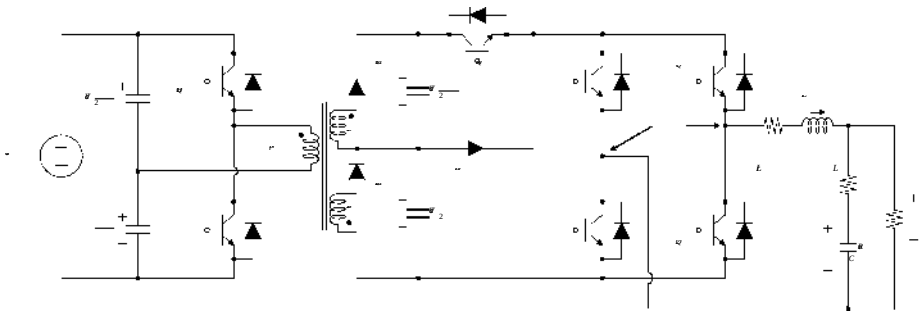


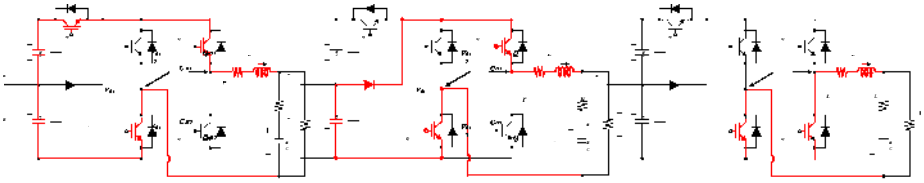
Fig. 1. Circuit configuration of the proposed multilevel inverter generating five levels on an output voltage wave.

Fig. 1 shows a circuit configuration of the proposed multilevel PWM inverter, which consists of a front-end Half-bridge converter connected to the primary of the transformer, series-connected capacitors, a switch, a diode, and H-bridge cell. It is designed to generate five levels on an output voltage wave. It needs a single dc input voltage source (V_{dc}), which is divided into two capacitor voltages. Each capacitor voltage becomes a half of the input voltage ($V_{dc}/2$), and it delivers energy to the secondary of the transformer, which has 1:1 turns-ratio. Diode D_A plays a role to synthesize $V_{dc}/2$ level to the output voltage, and a switching device Q_A supplies V_{dc} level to the output. Switches in an H-bridge cell works to determine the polarity of the output voltage and chopping the output voltage wave in order to make an output voltage near to a sinusoidal wave after low pass filtering (LC). By employing a transformer, it ensures a galvanic isolation between input and output. Voltage unbalancing problem usually occurred in series-connected capacitors are solved by controlling of Q_H and Q_{HB} at a front-end Half-bridge. Compared with a conventional cascaded H-bridge multilevel inverter when generating 5-level on an output voltage wave, the proposed approach reduces switching devices required to generate voltage levels up to three, and moreover, it just uses a single dc voltage source. In Fig. 1, the proposed approach employs an output filter consisted of inductor and capacitor to obtain a sinusoidal wave. Here, it considers on equivalent series resistances (r_L and r_C).

2.1 Operational modes

The operation of the front-end half-bridge converter is exactly same to the conventional one. When $_{QH1}$ turns on, voltage across $_{CH1}$ is applied to the primary of the transformer, and then energy in $_{CH1}$ is transferred to the upper capacitor $_{(CM1)}$ of the secondary. When $_{QH1}$ turns off, $_{QH2}$ works to charge the lower capacitor $_{(CM2)}$ of the secondary. By controlling of duty-ratio of these two primary switches, it can maintain voltage across each capacitor in a constant value ($V_{dc}/2$). So voltage unbalance problem usually occurred at series-connected capacitors can be solved in an easy way.

To help reader's understand, we explain operational modes, which is required to synthesize output voltage levels in the proposed inverter. Here, we explain that the polarity of the output is positive. In a case of a negative output voltage, working switches in an H-bridge cell are changed from Q_1, Q_4 to Q_2, Q_3. Fig. 2 shows three operational modes generating $_{Vdc,}$ $V_{dc}/2$, and *0*. Switch Q_A and diode D_A play important roles to generate $_{Vdc}$ ^{and} $_{Vdc/2}$ levels. When Q_A turns on, voltage across the series-connected capacitors appears on $_{vAB}$ as shown in Fig. 2(a). To produce $V_{dc}/2$ level, Q_A turns off, and then voltage across the lower capacitor appears on $_{vAB}$ via D_A as shown in Fig. 2(b). During the mentioned two modes, Q_4 maintains on-state, and Q_1 iterates on and off for generating pulse width modulated waves. Zero level can be made by two methods based on voltage cancellation. Here, Q_2 and Q_4 turn on at the same time as shown in Fig. 2(c).



(a) (b) (c)

Fig. 2. Operational modes, (a) *Vdc* level, (b) *Vdc/2* level, (c) *0* level.

2.2 Switching scheme

Basic principle of switching strategy is to generate gate signals by comparing a reference signal with two carrier waves having same frequency and phase, but different offset voltage. When the modulation index is less than 0.5, the lower carrier wave (*Carrier_B*) is compared with a reference signal. Hence, the switching components in an H-bridge cell of the proposed inverter is identical to conventional full-bridge inverter, and the harmonic contents in an output voltage is equal to that of conventional inverter. When the modulation index is greater than 0.5, both *Carrier_A* and *Carrier_B* are compared with a reference signal. Here, the switching function produced by *Carrier_A* is prior to *Carrier_B*. According to the amplitude of the reference, the operation interval of each mode varies within a certain period. The period of each mode is determined by

Mode A: and . (1)

Mode B: . (2)

Mode C: and . (3)

Mode D: . (4)

The phase angle is dependent on the modulation index *M*. The modulation index of proposed 5-level inverter is defined as

—— . (5)

where A_C is a peak-to-peak value of carrier wave, and A_M is amplitude of a reference voltage $_{(vref)}$. Therefore, when the modulation index is less than 0.5, the phase angle displacement is equal to (6).

and . (6)

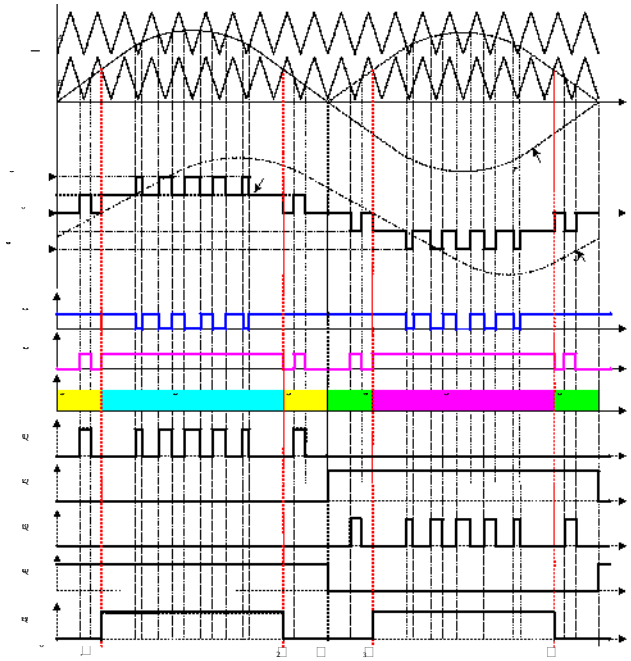


Fig. 3. Switching pattern for the proposed 5-level PWM inverter.

On the other hand, when the modulation index is higher than 0.5, the phase angle displacement is determined by (7) through (10).

. (7)

.

(8)

(9)

. (10)

As shown in Fig. 3, the control signals are generated by the signals (C_A, C_B) come from comparators which compare the respective carrier signal and the voltage reference $_{vref,}$ the signals S_1 - S_6 are produced by the phase angle displacement. The switching functions of proposed inverter are expressed by using logical AND, OR, NOT gates.

. (11)

. (12)

. (13)

. (14)

. (15)

The output voltage produced by comparison of a reference and two carrier waves can be given in Fourier series by (16).

. (16)

If there are P pulses per 1/4 period and P is an odd number, the coefficients B_n and

A_0 would be a zero where n is an even number. Therefore, (16) can be rewritten by (17).

. (17)

where m is a pulse number. Total harmonic distortion (THD) and distortion factor (DF) are defined as

. (18)

(19)

(20)

High order harmonic components can be easily eliminated by a low-pass filter at the output stage.

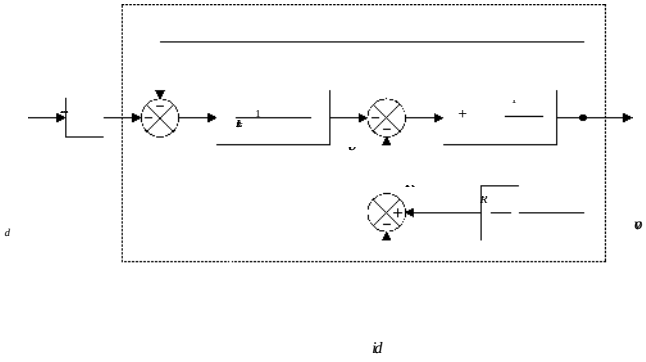


Fig. 4. Control block diagram of proposed five-level PWM inverter.

Fig. 4 shows a control block diagram of the proposed five-level PWM inverter. From this control diagram, we describe a linear model of the proposed inverter in (21).

(21)

(22)

The system response depends upon the pole of transfer function. A good dynamic response can be obtained by shifting the position of the pole as closer as left side in the s-plane.

3 Simulation Results

Generally, it is important that harmonics of output voltage produced by inverter itself should be reduced to alleviate the output current ripple and core loss of inductor. For this purpose, computer-aided simulation is performed to prove availability of proposed 5-level PWM inverter. Fig. 5 shows the simulated waveforms of output

voltage, current and its harmonic components by FFT analysis when the modulation index is 0.6. It can be shown in this figure that THD and DF in the proposed inverter are 0.37[%] and 0.01[%]. When the modulation index is higher, THD and DF of the proposed inverter will slightly increase. It is a matter of cause because the larger the value of *M* being increased, the smaller the regions of half-level of dc bus voltage are reduced. Fig. 6 shows the effect of the modulation index *M* on the THD and DF for the conventional 3-level PWM inverter and the proposed five-level PWM inverter. It is clear that the harmonic components of the proposed inverter can be considerably reduced.

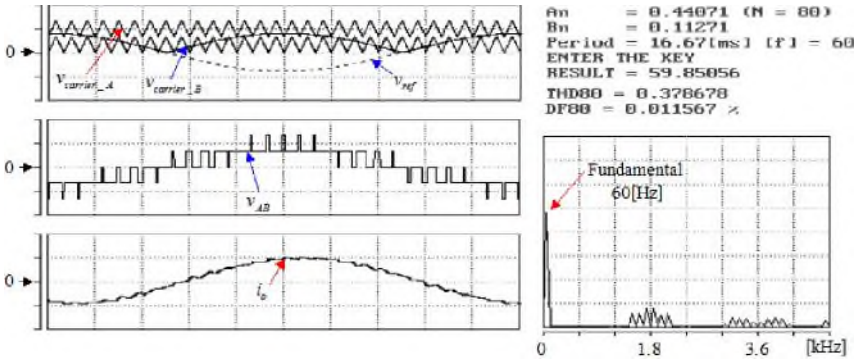
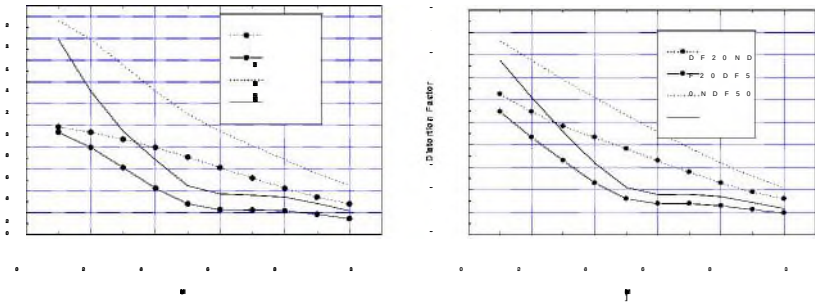


Fig. 5. Simulation results of output voltage, output current, and FFT.



(a) (b)

Fig. 6. Comparison of THD and DF variation, (a) total harmonic distortion, (b) distortion factor.

4 Conclusions

In this paper, we proposed a five-level PWM inverter using an isolated Half-bridge circuit configuration. Compared with a conventional cascaded H-bridge multilevel

inverter synthesizing five-level on output voltage wave, the proposed approach generates the same voltage levels using an isolated Half-bridge configuration adding a switching device and a diode. Additionally, it just employs a single dc voltage source whereas the conventional approach needs two independent dc voltage sources. Moreover, it improves reliability and stability by applying a transformer ensuring a galvanic isolation between a dc voltage source and the output. After theoretical analysis, we carried out a computer-aided simulation to prove the validity of the proposed approach.

Acknowledgments. This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2012R1A1A2006120).

References

1.Abu-Rub, H., Holtz, J., Baoming, Ge: Medium-Voltage Multilevel Converters-State of the Art, Challenges, and Requirements in Industrial Application. IEEE Trans. Ind. Electron., 57, 2581--2596 (2010)
2.Rodriguez, J., Bernet, S., Bin Wu, Pontt, J.O., Kouro, S.: Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives. IEEE Trans. Ind. Electron., 54, 2930--2945 (2007)
3.Jin-sung, C., Feel-soon, K.: Five-level inverter using modified H-bridge circuit congiguration. In: KIEE annual conference, pp. 259—261. KIEE Press, Korea (2012)
4.Feel-soon, K., Sung-jun, P., Man-hyung, L., Cheul-U, K.: An efficient multilevel-synthesis approach and its application to a 27-level inverter. IEEE Trans. Ind. Electron., 52, pp. 1600-1606 (2005)
5.Ounejjar, Y., Al-Haddad, K., Grégoire, L.A.: Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation. IEEE Trans. Ind. Electron., 58, pp. 1294--1306 (2011)
6.Ebrahimi, J., Babaei, E., Gharehpetian, G.B.: A New Multilevel Converter Topology With Reduced Number of Power Electronic Components. IEEE Trans. Ind. Electron., 59, pp. 655-667 (2012)
7.Babaei, E.: A Cascade Multilevel Converter Topology with Reduced Number of Switches. IEEE Trans. Power Electron., 23, pp. 2657--2664 (2008)
8.Najafi, E., Yatim, A.H.M.: Design and Implementation of a New Multilevel Inverter Topology. IEEE Trans. Ind. Electron., 59, pp. 4148--4154 (2012)
9.Youhei, H., Hirotaka, K.: A Single-Phase Multilevel Inverter Using Switched Series/Parallel DC Voltage Sources. IEEE Trans. Ind. Electron., 57, pp. 2643--2650 (2010)

