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Hardware/Software Codesign - HS 15

Exercise Sheet 3

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3.1 Specification Graph

Fig. 1a) shows a task graph, and Fig. 1b) the available architecture to implement it. The four tasks of the task graph, T1 ... T4, can be executed on different components of the target architecture, as defined by Table 1.

Component	Binding			
	T1	T2	T3	T4
MIPS	✓	—	—	✓
DSP	—	✓	✓	✓
FPGA	—	✓	✓	—
ASIC	—	—	✓	—

Table 1: Possible bindings for tasks T1 ... T4.

3.1.a) Architecture Graph

Construct the problem graph for the task graph in Fig. 1a) by inserting communication nodes. Construct the architecture graph for the target architecture in Fig. 1b).

3.1.b) Specification Graph

Construct the specification graph. Which constraints for the binding and the allocation can be seen? Modify the target architecture to get more implementation alternatives.

3.2 Clustering

Generate partitions for the graph in Fig. 2 by hierarchical clustering.

The edge weights in Fig. 2 denote the closeness between the objects. For computing the closeness values of the newly inserted edges to the hierarchical clusters use:

- (a) the average value
- (b) the minimum

of the closeness values before the clustering.

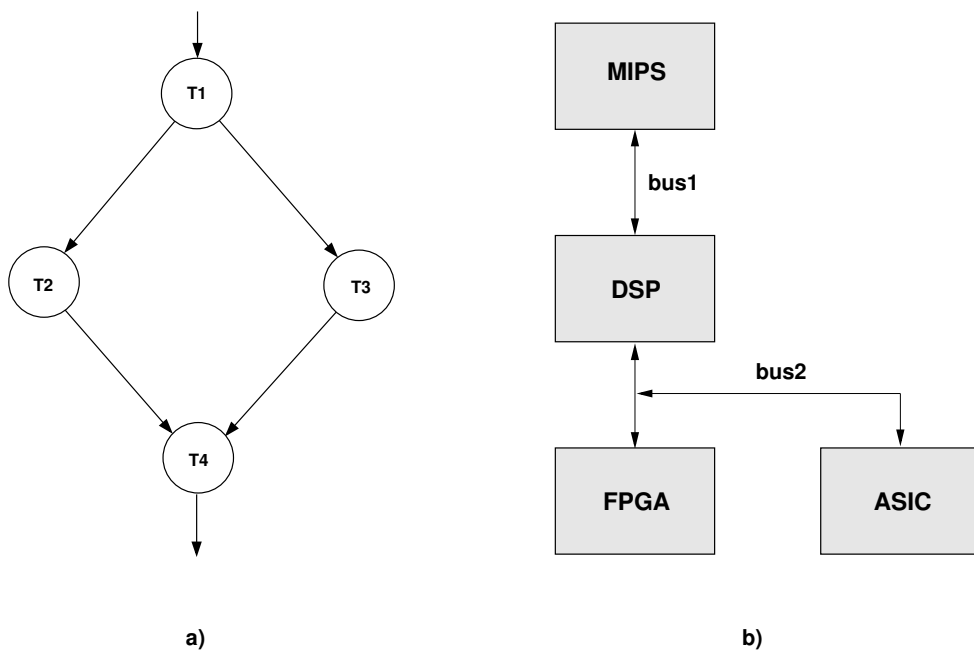


Figure 1: Task graph and target architecture

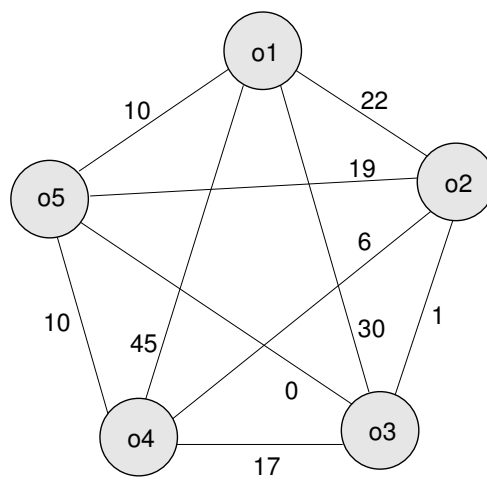


Figure 2: Graph with objects