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Design of a 0.97dB, 5.8GHz fully integrated CMOS low noise amplifier

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Abstract. This paper presents a 5.8 GHz fully integrated CMOS low noise amplifier (LNA) with on chip spiral inductors for wireless applications. Simulation results show that the noise figure (NF) of the proposed LNA at 5.8 GHz central frequency is only 0.972 dB, which is perfectly close to NFmin while maintaining the other performances. The LNA also has a power consumption of 6.4 mW, a gain of 17.04 dB, and an input 1-dB compression point $_{(IP1dB)}$ about -21.22 dBm while at 1.8V supply voltage. The proposed LNA topology is very suitable for IEEE 802.11a, 802.11n wireless applications.

Keywords: CMOS, low noise amplifier, noise figure, power consumption

1 Introduction

During the recent years radio frequency (RF) and microwave electronics have faced with the following major advances: the boom of telecommunications market; a rise in application frequency; the emergence of silicon-based processes in the microwave area [1]. Moreover, the widely application of the high-speed (up to 54Mb/s) wireless local area network (WLAN), which makes all kinds of portable wireless communication products have considerably developed and the demands for higher frequency band, faster transfer rates and wider bandwidth RFIC has also rose sharply in consumer electronics market. Some WLAN standards such as IEEE 802.11a (5-5.825GHz), IEEE 802.11n (2.4-2.485GHz and 5.725-5.825GHz) and U-NII (5.15-5.35GHz and 5.725-5.825GHz) require a transceiver with approximately 5.5GHz center frequency [2].

In millimetre-wave receiver design, the low-noise amplifier (LNA) is a critical building block that amplifies the received signal and contributes most of the noise figure of the whole receiver [3]. In order to replace the external off-chip LNAs with CMOS LNAs, the noise figure (NF) less than 1dB is required with lower consumption. Adding in progressively lower power dissipation constraints inherent to battery-powered portable applications, a primary challenge in LNA design is achieving simultaneous noise and input matching at any given amount of power dissipation. Moreover, the amplifier's compression point requirement also imposes a limitation on the LNA transistor size, making the simultaneous noise and input match even more difficult to achieve in practice [4]. Therefore, many kinds of amplifier topologies have

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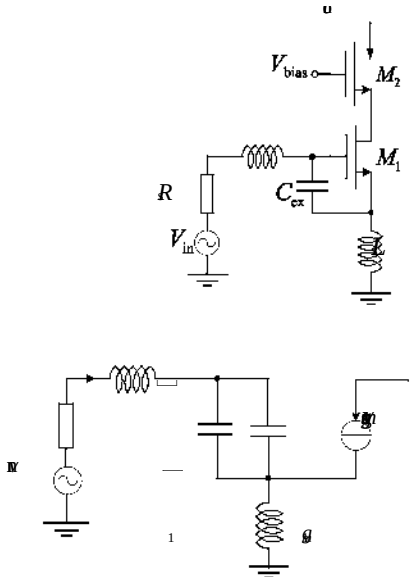
been proposed as a way to satisfy the requirement for low power dissipation as well as good performances. In this paper, a 0.18μm CMOS LNA simultaneously achieving input impedance and minimum noise matching, and excellent noise figure has been designed, which is suitable for IEEE 802.11a, 802.11n wireless applications.

2 Circuit design and analysis

2.1 Topology

Fig.1 (a) shows the traditional cascode structure with the inductive source degeneration. Its small signal equivalent circuit is shown in Fig.1 (b).



(a) *(b)*

Fig.1. (a) The cascode LNA with inductive degeneration; (**b**) Small signal equivalent circuit of Fig.1 (a).

$$R_s$$

$$i_x$$

$$g_L$$

$$C^{g_L}$$

ex

A capacitor is connected between gate-source of the input transistors M1 to achieve noise and input match simultaneously [3]. This well-know structure is widely used due to its high gain and the increase in the output impedance as well as better isolation between the input and output ports. The input impedance of this LNA can be equal to (1), in which the gate resistance and the total parasitic capacitances except gate-source capacitances are neglected to simplify the analysis.

(1)

Where and are the intrinsic gate-to-source capacitor and the transconductance of M_1, respectively. When the input impedance matching network composed by , and resonating at the operating frequency, the imaginary part of is eliminated. The impedance becomes a pure real part and only relevant to and , Therefore, by adjusting and can easily realize to real 50 resistance at the input of the LNA.

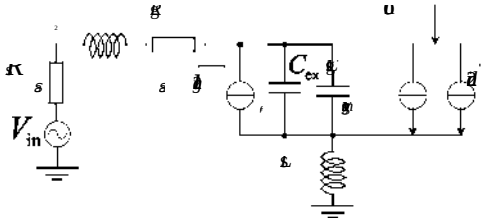


Fig.2. The small signal noise equivalent circuit of the input stage.

2.2 Noise analysis

Fig.2 is the simplified small signal noise equivalent circuit. Because the derivation of the complete noise figure equation (taking into the effect of all existing parasitics in the circuit) would be quite cumbersome, and the obtained results would not give an insight into how to choose design parameters such as the width and the biasing of the transistors. Therefore, if the noise contribution from the cascode stage is ignored, the noise factor of the cascode LNA becomes [5, 6]

$$z = 1 + 2cQ$$

$$Q_{in}$$

$$C_{ex}$$

$$F = \frac{R}{R} \quad \frac{}{a} \quad \frac{}{1} \qquad (2)$$

$$\left| \right| \sqrt{L_g} \qquad (4)$$

$$\omega \qquad (5)$$

Where is the input voltage source resistance, is the gate resistance of M_1, is the operating frequency, , and are bias-dependant parameters. The inductive source degeneration is employed to make (where is the complex conjugate of the amplifier input impedance) close to , as derived in Eq (5).

(5)

Where is the optimum noise impedance. Note that in equation 2 the second term shows the noise due to the gate resistance, which can be minimized by careful layout techniques, by increasing the number of fingers in the design we can effectively reduce this resistance. Therefore, the only term which is of our concern should be optimized is the third one. Based on the methodology in [3], simultaneous input impedance and noise matching at 5.8GHz frequency are achieved by appropriately selecting the values of , , and the size and bias of the input transistor M_1. Nevertheless, to reach simultaneously noise and power exactly matching at power constrained condition is a very difficult job in practice. Because that the LNA design involves trade-offs between noise-figure, gain, power dissipation, input matching, and harmonic content in the output signal. In this circuit, the capacitor is a key component, which has a great effect on NF and the available power gain of the LNA. Too much will lead to noise and gain deterioration due to the degradation of the cutoff frequency of the composite transistor . Fig.3 and Fig.4 show the relationship between the different capacitance and NF and gain, respectively.

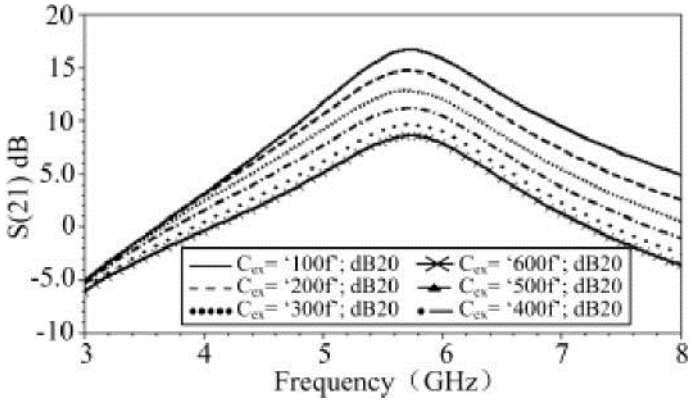


Fig.3. The relationship between the capacitance and the gain .

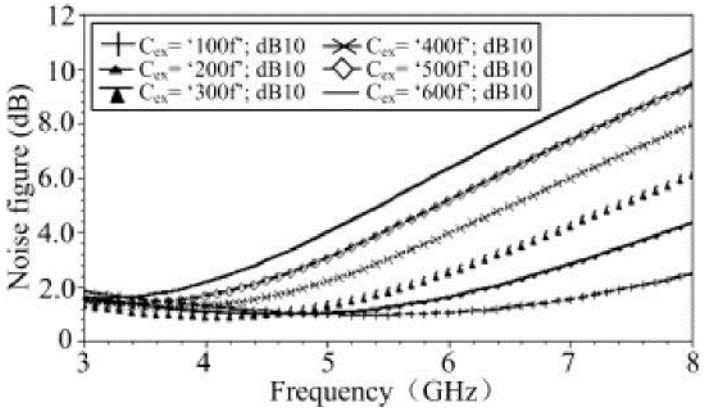


Fig.4. The relationship between the capacitance and the noise .

Therefore, in this work, based on the traditional cascode structure as analysis above, we propose a LNA schematic as shown in Fig.5.

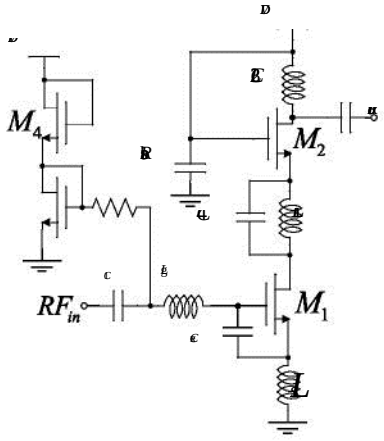


Fig.5. Complete schematic of the LNA.

*C*2

M 3

In this circuit L_1, C_4 are inserted between the cascade transistor M_1 and M_2 for inter-stage matching to improve the LNA gain and noise performance. Transistors M_3, M_4 are used to bias the LNA by mirroring the reference current to the transistor M_1. The value of the bias resistant R_{bias} is about 2~4k , which can avoid the signal path disturbed by the biasing circuit and mitigate the effect of gate-source capacitance of

the transistor M_3.

3 Simulation results and discussions

The LNA has been designed in a TSMC 0.18-μm RF technology with the help of

Cadence Spectre RF. The lengths of all the transistors adopt the minimum channel length 0.18μm to obtain a higher cutoff frequency. The main component parameters of the LNA are listed as follows: the overdrive voltage of M_1 is 81mV, the gate-width of M_1 and M_2 are 134.9μm. Using a supply voltage of 1.8V, the designed LNA including the bias circuit draw only 3.56mA resulting in a power consumption of 6.4mW. This is relatively low for a 5.8 GHz CMOS differential LNA with a power gain greater than 17.04 dB. The complete simulations of the designed LNA are shown in Figs 6 to 9 and in Table 1.

Fig.6 shows the simulated scattering parameters of the LNA. In the operating frequency of 5.8GHz, a power gain of 17.04 dB is achieved. The input return and output return losses (,) of the LNA are -17.46 dB and -22.4dB at 5.8GHz, respectively. Reverse isolation is -28.3 dB; that good reverse isolation is due to utilizing cascade structure.

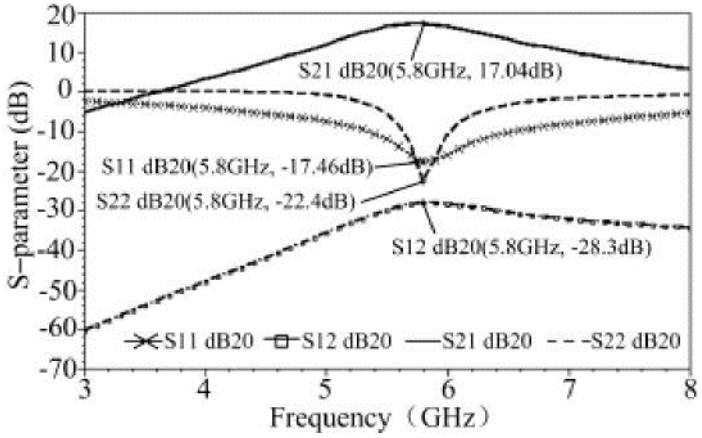


Fig.6. Simulated S-parameters of the LNA.

Fig.7 shows that the proposed LNA achieves a noise figure 0.9719 dB at the central frequency 5.8GHz, and with a NF ripple of 0.01 dB in the frequency range of 5.25-5.825GHz, which is excellent compared to recently reported designs. Note that, the NF of the LNA coincides with =0.9506 dB very well at the frequency of 5.8 GHz. The results illustrate that the noise matching has met the requirement. Fig.8 shows the simulation result of the input 1-dB compression point $_{(IP1dB)}$. An input sinusoidal signal with a frequency of 5.8 GHz is used. The value of $_{IP1dB}$ is about -21.22 dBm.

Besides, it has been shown that stability factor K_f>1 (or Bf>0) alone is necessary and sufficient for a circuit to be unconditionally stable [7]. Fig. 9 shows the simulate stability factors K_f and B_f versus frequency characteristics of the LNA. The LNA meets the unconditional stability requirement over a range of 3–8 GHz.

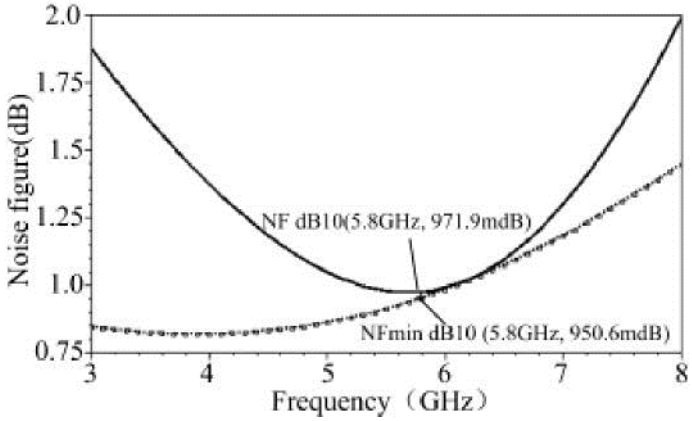


Fig. 7. The simulation of noise figure.

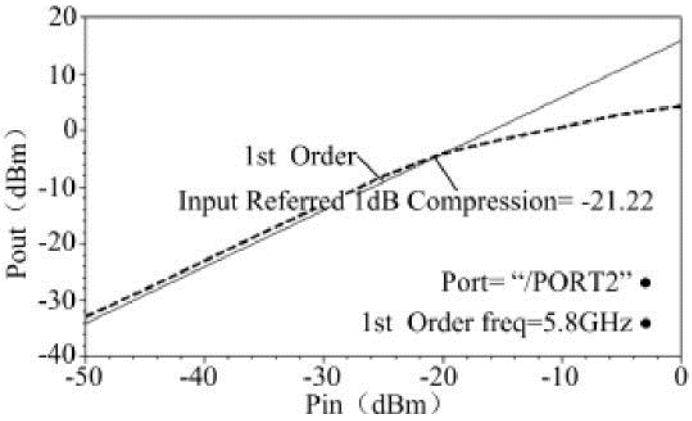


Fig.8. The simulation result of the input 1-dB compression point.

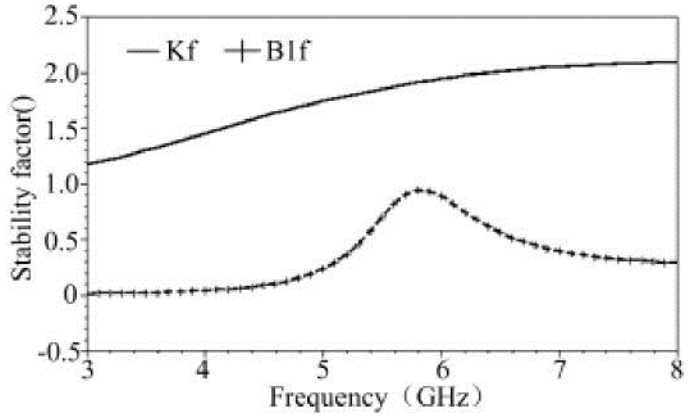


Fig.9. Simulation result of the LNA stability.

Table.1 summarizes the performance of the proposed CMOS LNA compared to the recently reported literatures. As can be seen from table1, the proposed LNA achieves a lower noise figure, a higher voltage gain and a smaller power dissipation compared to prior techniques listed. These results demonstrate that the proposed LNA is suitable for IEEE 802.11a, 802.11n wireless applications.

Table 1. Comparison between this work and other reported literatures.

Ref.	Tech.	Freq (GHz)	NF(dB)	Pdc(mW)	S21(dB)	S11/S22(dB)
[1]	0.35μm BiCMOS	5.8	3.0	3.8	12.1	- 20.7/-9
[2]	0.18μm (CMOS)	5.5	3.12	3.0	20.63	- 29.5/-25
[4]	0.18μm SOI	5.0	0.95	12.0	11.0	- 33/-
[8]	0.25μm (CMOS)	5.745	5.48	6.12	24.6	- 17.3/-5.3
[9]	0.18μm (CMOS)	5.8	2.0	16.0	14.1	<- 10/-11
[10]	0.18μm BiCMOS	5.8	2.0	32.4	18.8	<- 10/<-10
This work	0.18μm (CMOS)	5.8	0.97	6.4	17.04	-17.5/- 22.4

4 Conclusion

In this work, we present a 5.8GHz fully integrated LNA design and simulation using TSMC 0.18μm RF process. The cascade topology was chosen for this design as it offers higher power gain, better reverse isolation and reduces miller effect. Simulation results have shown that the proposed LNA circuit consumes only 6.4mW from a 1.8V supply voltage while achieving a power gain of 17.04 dB, a excellent noise figure 0.972dB at the operating frequency 5.8GHz. Considering the performance achieved, the proposed techniques demonstrate to be very suitable for the implementation of narrowband LNAs in wireless receivers.

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