Microscopic Analysis of Chips: Chips deprocessing

Dominik Malë´ık and Martin Drahansk´y

Faculty of Information Technology, Brno University of Technology, Bo˘zetëchova 2, 61266 Brno, Czech Republic
{imalcik,drahan}@fit.vutbr.cz
http://www.fit.vutbr.cz

Abstract. Nowadays many different types of chips are used virtually everywhere in the real world. Sometimes, it is necessary to ensure that a certain chip meets specific requirements. For this reason, it is essential to examine various properties of chips; one of those can be, e.g., the chip security with respect to its physical structure.
This paper is a sequel to our previous publication regarding chip decapsulation. A further process of chip deprocessing is presented, so that the reader should be able to decapsulate a chip and also reveal the secrets of bare transistors hidden under different layers. The obtained specimens can be analysed with use of a microscope. Main analysis of such specimens will be the target for our next work.

Key words: microscope, chip, chip package, leadframe, decapsulation, bare chip, chip deprocessing, analysis of chips

1 Introduction

The current trend is increasing constantly the concentration of different electronic systems. These can be found, without exaggeration, almost everywhere. In certain situations, we expect a definite level of security or specific features in general to be guaranteed. We are therefore always forced to invent new ways to provide all the needed properties of these chip modules. The new methods have to be analysed and tested properly.

This article is the result of our effort to develop semiautomatic application and related methodologies to support the chips analysis and testing. Our previous work focused on the first phase of the whole analysis process – the decapsulation process. The decapsulation process has been described in detail. In the case of interest to obtain chips from PCBs *(Printed Circuit Board)* or in the main decapsulation process, we recommend to read the paper [2].

Currently, we are able to obtain bare chips from different types of plastic packages. Moreover, this paper presents further steps in chips deprocessing and gaining of desired pictures of bare transistor layers. With such an ability we will go on working on the main analysis of the transistor layers[1].

[1] New results of transistor layers analysis will be presented in our next paper.

2 Chip decomposition

Each modern chip is a composition of different layers with different functions. Layers are made of particular compounds with respect to the desired functionality. Using an ordinary grinder can result in a destruction of a processed specimen, because the layers are very thin and so it is sometimes very difficult to determine the correct time frame of grinding. In addition, it is also very difficult (and sometimes almost impossible with an ordinary lab grinder) to keep the whole chip surface in an absolutely same level to polish exactly the same amount of compound in each point of the surface to achieve the precise result.

Apart from using a grinder to remove the layers, there is a chemical way of removing particular layers. We would like to introduce two methods based on one chemical approach in the following text. Let us name the processes as a *reduced process* and a *complete process.* As the processes' names reveal, the reduced process can be understood as some kind of subset of the complete process.

2.1 Reduced process

The reduced process jumps directly to the decomposition of the chip without any knowledge of its composition. This may seem to be inconvenient, however, for our purposes, it is mainly sufficient to apply this approach, because of a typical composition scheme employed by chip producers. This method can be considered as a type of trial and error method. The researcher simply tries to use removal methods for particular layers in a common or in a predicted order. The method is really feasible due to the fact that in the case of a wrong removal method choice, virtually nothing happens – the wrong method simply does not react with an inappropriate layer. Nevertheless, the researcher still has to be very careful, because the incorrectly chosen removal method can still react with the appropriate layer edge that is usually exposed on the border of the chip and so the current top level layer can be under-etched.

For purposes of making experiments it is convenient to use this method. It is also assumed that a sufficient amount of chips of the same type is available. The process relies on the fact that the first layer is usually some kind of passi-vation and so an appropriate removal method should be applied. A conductive layer composed of aluminium compounds usually follows. An insulant layer (oxide compounds) should be present to separate another conductive layers. These conductive and insulant layers then usually alternate down to the silicon layer.

The mentioned approach can be used for many of the contemporary chips (we have successfully applied this reduced method to different RFID chips). For some chips it is necessary to experiment also with incorporating plasmatic etching or even with an absolutely different removal method at some point of the decomposition process because of the presence of a different layer type. It is strongly recommended to investigate the deprocessing results after each particular procedure to avoid any unwanted damage of the chip.

2.2 Complete process

The complete process is recommended in the case of us not having a sufficient amount of the same type of chips, because it incorporates an analysis regarding the layers' composition. For this analysis it is necessary to have at least one specimen of the chip. At least another one piece is needed for the main deprocessing.

The complete process is usually recommended for situations when a precise decomposition is necessary in the first attempt of the deprocessing. As mentioned earlier in this chapter, it is needed to have at least two specimens – the first one has to be sacrificed for the material composition analysis (cross-section analysis) of particular layers and the second one can be then deprocessed according to the information gained from the first step.

Cross-section analysis Let us assume that a bare chip is available for further steps[2]. A suitable grinder is needed for making a specimen cross-section. It is not necessary to have a specific type of a grinder, but it is rather important to be able to obtain the chip cross-section.

After the cross-section has been made, the next step is to employ one of the spectrometric techniques to acquire the elements' composition. For example an electron microscope equipped with an X-ray detector can provide such information. Afterwards, a precise deprocessing procedure can be prepared according to the composition and thickness of each layer. This can obviously result in a very precise scheme of the main decomposition.

The main deprocessing With the outcome of the cross-section analysis, an exact sequence of particular steps can be performed in order to get the coveted deprocessed chip. The form of the whole process naturally depends on our objectives. Usually, a picture of bare transistors is desired, however, it is not a rule. Therefore, the process can be sometimes completely different, e.g. just to get rid of the first passivation layer or to obtain pictures of all conductive layers, etc.

2.3 Common layers deprocessing

According to the information given in chapter 2.1, the decomposition process usually consists of a specific sequence of particular steps. The most common layers and matching chemical procedure are described below. The correct combination of actions is naturally dependant on the chip type.

Passivation The very first layer is mostly a passivation. To remove this layer type, it is recommended to use plasmatic etching. The whole process takes about 45 minutes with our old plasmatic etcher TESLA 214 VT, but the actual plasmatic etching lasts only 4 minutes out of the mentioned time

[2] The process of obtaining bare chips is dealt in our previous work [2], [1].

period (the length of plasmatic etching process depends on the type of plasmatic etcher and should be adjusted according to the particular machine performance). The rest of time is devoted to prepare conditions necessary for performing this procedure.

Aluminium compounds Conductive layers made of aluminium compounds can be taken away by application of *phosphoric acid etching mixture, PEWS 765-140-57-36* [3]. The recommended working temperature is 50 °C, the common time of bath should be from 2 to 6 minutes.

Oxide compounds A special chemical mixture is available also for removing oxide compounds. Precisely, the mixture consists of ammonium fluoride and hydrofluoric acid in ratio 7:1. The working temperature is 30 °C, the common time of bath should be from 2 to 6 minutes.

3 Results

Just to illustrate our research, let us introduce two figures. The first one depicts differences between decapsulated chip with a preserved passivation layer (see the left part of Fig. 1) and the same specimen after five steps of decomposition process (see the right part of Fig. 1) – 4 minutes of plasmatic etching (passivation); 4 minutes of etching – use of PEWS (aluminium compounds); 4 + 2 minutes of etching – use of ammonium fluoride and hydrofluoric acid in ratio 7:1 (oxide compounds); 5 minutes of etching – use of PEWS (aluminium compounds); 3 minutes of plasmatic etching (removing the last layer above transistors).

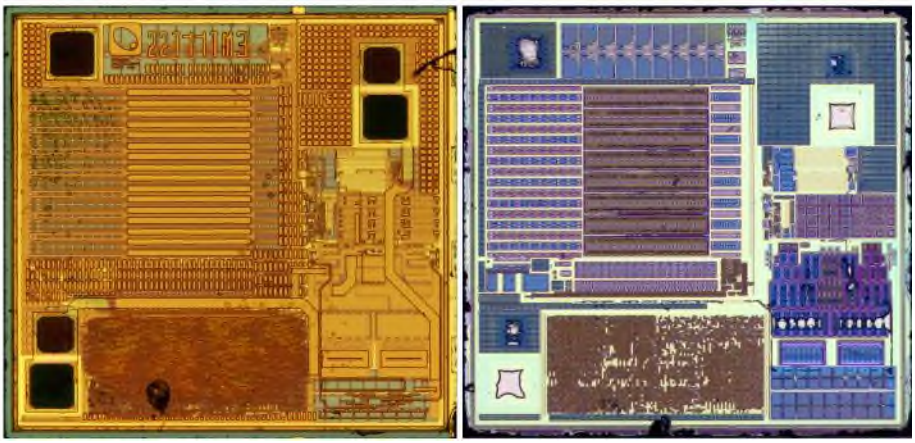

Fig. 1. Two images of MIFARE classic 1KB. The decapsulated chip without any application of decomposition (left). The same chip after several steps of deprocessing (right).

[3] http://www51.honeywell.com/sm/em/common/documents/2.6 europe msds p 8. pdf

The second picture shows the final result of our effort – bare transistors prepared for the analysis (see Fig. 2). It is obvious that the image quality is not ideal, because of limitations of optical microscopy. We intend to use an electron microscope for the future work. This will assure sufficient image quality.

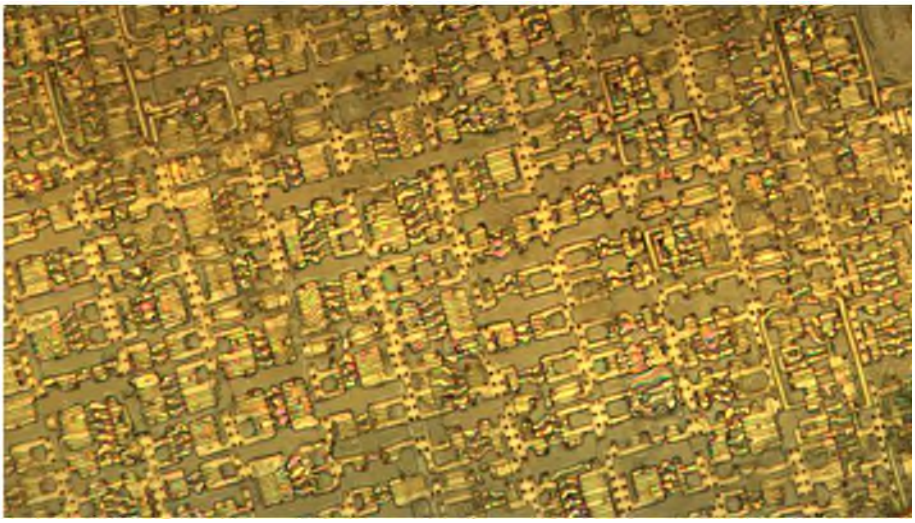

Fig. 2. The detail of an RFID tag – bare transistors can be recognised. This image was acquired by optical microscope Olympus BX61 with insufficient magnification abilities; our intention is to use an electron microscope to obtain better quality images for analysis.

4 Conclusion

The outcome of our effort that has been exerted during the last year is presented was this paper. We are now about to start making the main part of the microscopic analysis of chips (in fact, we have already started with RFID and smart cards chips, but the results have not been evaluated yet). Specimens for the analysis can be now fully prepared at our department. This means that we are able to concentrate on the analysis itself and on the whole process improvement. As soon as the first evaluation of the analysis will be ready, the next paper will be prepared.

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